Stacking Fault Growth During SiC PiN Diode Operation

Robert Stahlbush
Naval Research Laboratory, Code 6813
4555 Overlook Ave. SW
Washington, DC 20375
tel: (202) 767-3357
e-mail: stahlbush@nrl.navy.mil

Background

- SiC advantages for power devices

  Larger bandgap 4H SiC: 3.2 eV Si: 1.1 eV
  higher breakdown field 10X larger
  higher breakdown voltages

  high electron bulk mobility
  high thermal conductivity

- Reports from ABB about forward I-V degradation

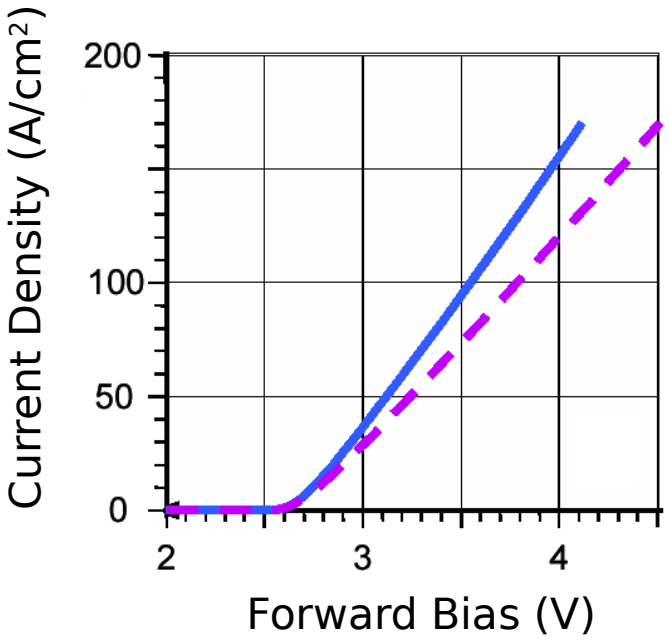
  Attributed to stacking faults

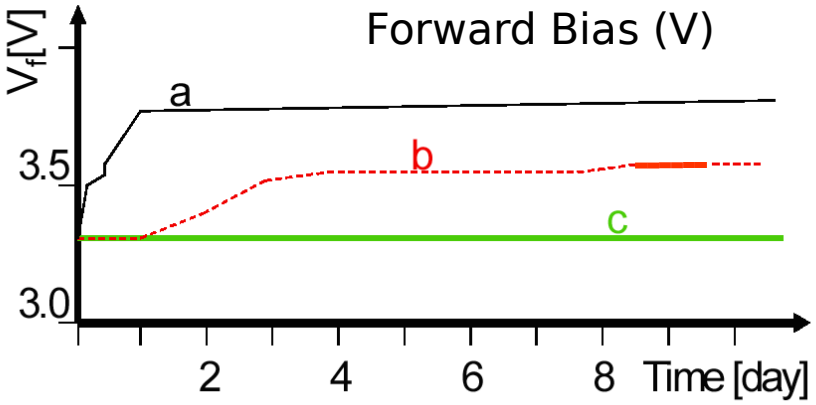
- Room temperature (< 100 °C) stacking fault formation

Stacking Fault Growth During Diode Operation

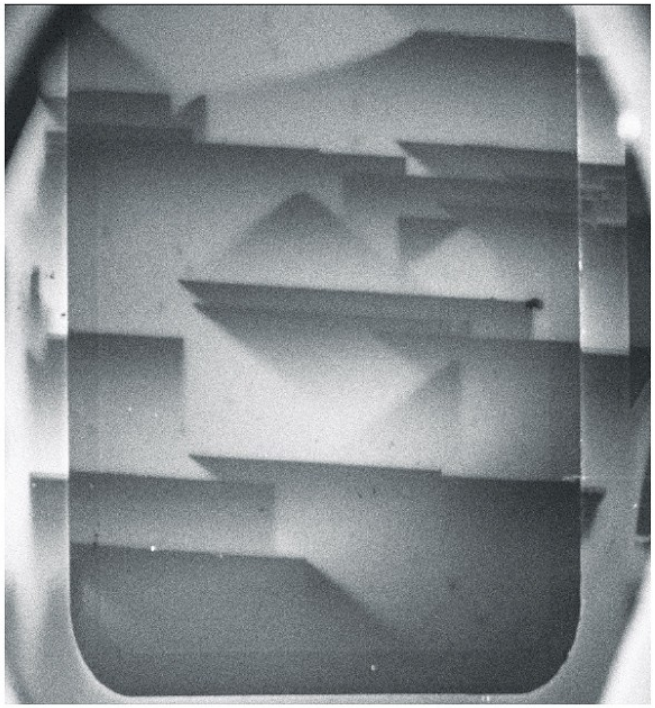
- Discovered by the power company ABB while developing SiC PiN diodes
- Forward-biased current degradation
- Went public after failing to solve the problem internally
- Critical problem - must be overcome before SiC bipolar devices are commercially or militarily viable

I-V Degradation due to Stacking Fault Growth





Stacking Faults After Stressing Diode



from Lendenmann, Bergman, Mater. Sci. Forum 353-356, 727, 299 (2001)

Physics of I-V Degradation

- How stacking faults degrade forward-biased current

  Quantum well
  Reduces minority carrier lifetime

- Stacking fault growth mechanism

  Nucleation site ??

  Driving force ??
  - stress in epi layer
  - lowering electronic energy (3C vs 4H)

  Activation energy
  - electron-hole recombination

Technical Approach

- Use light emission imaging to:
  - Characterize defect growth during device operation
  - Identify primary defects in reverse bias operation
- Use X-ray topography and site-specific TEM to determine defect crystal structure
- Link defect structure to defect source (e.g. dislocations, point defect condensation)
- Work closely with providers of state-of-the-art material and devices

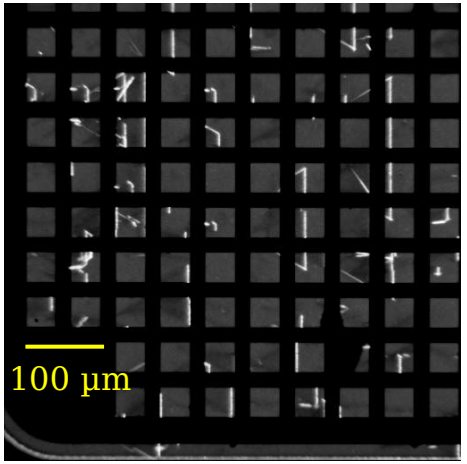
Characterization Approach

- Light Emission
  collected during device operation
  monitor I-V

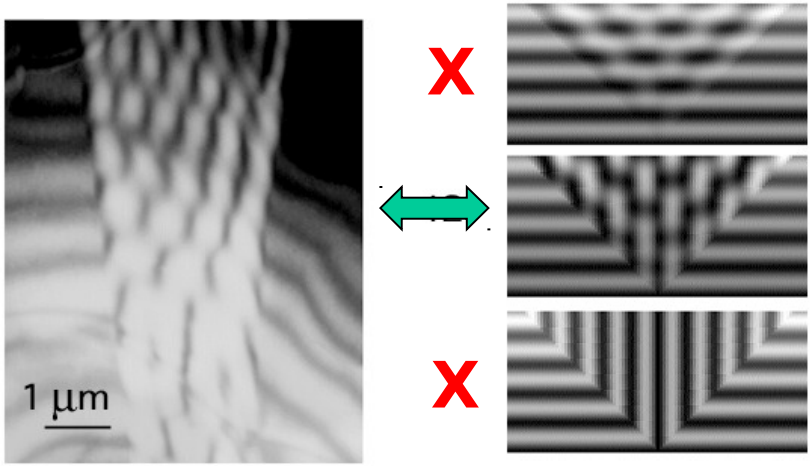
- X-ray topography
  non-destructive
  works with or without devices present

- Site-specific TEM
  atomic structrure of defects

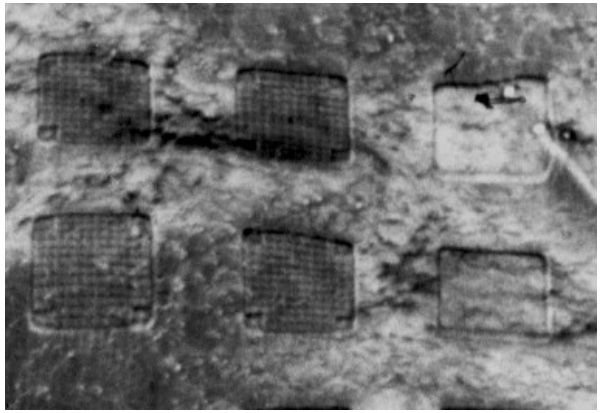
Light Emission from Dislocations



Site-specific TEM & Simulations



X-ray Topograph of Diodes



Industrial Collaborators

CREE

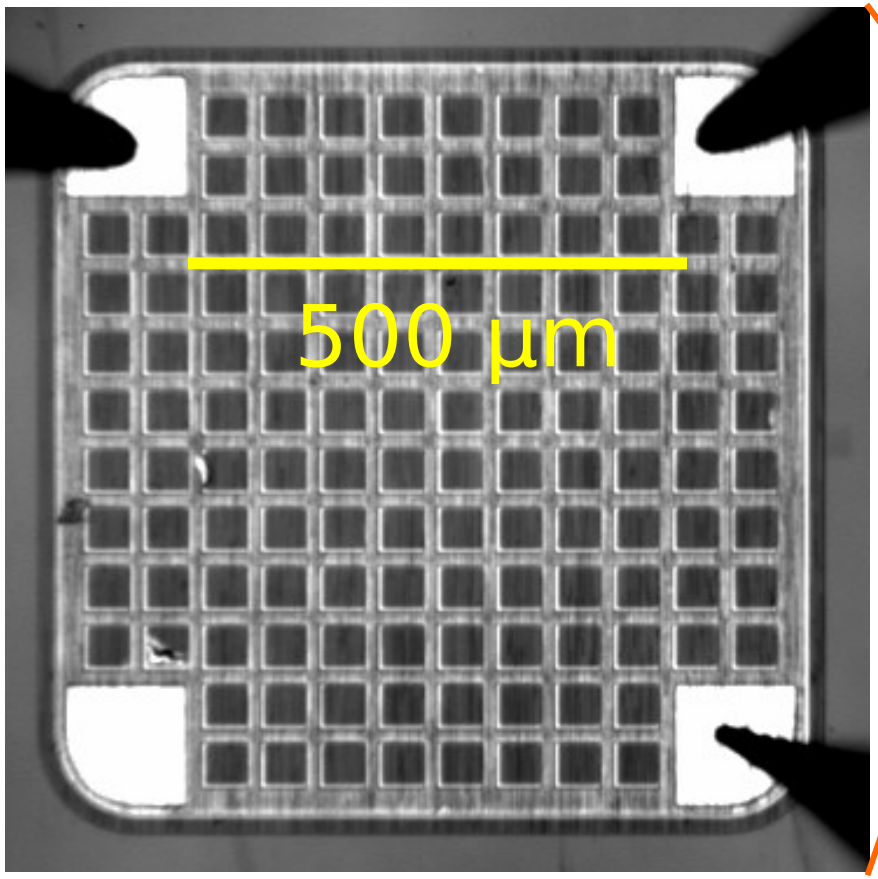
Rockwell

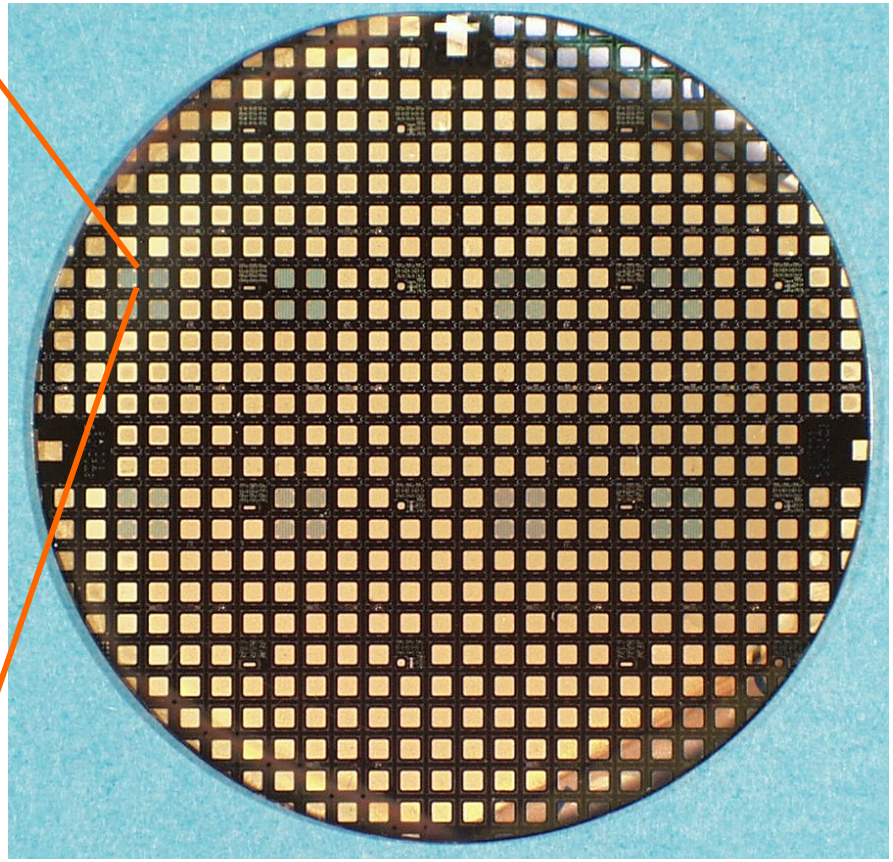
General Electric GRC

Sterling Semiconductor

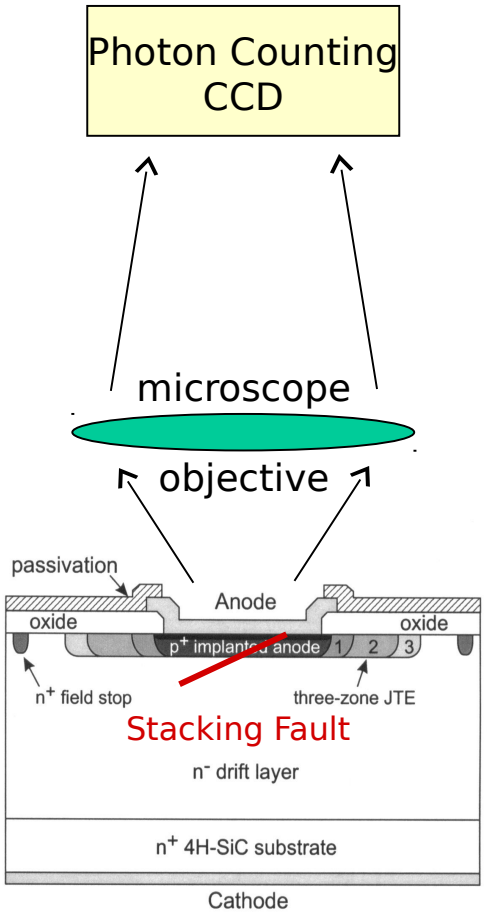
Light emission test structures included in wafers for SiC power devices

4H SiC Wafer with Fabricated PiN Diodes





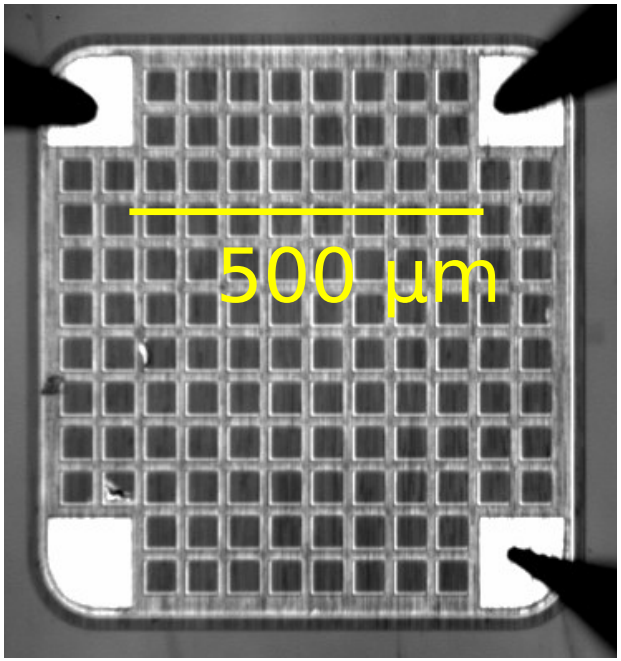
Diode Layout for Light Emission Imaging(LEI)



Cross Sectional View

Diode size 0.8 x 0.8 mm

Diode Image



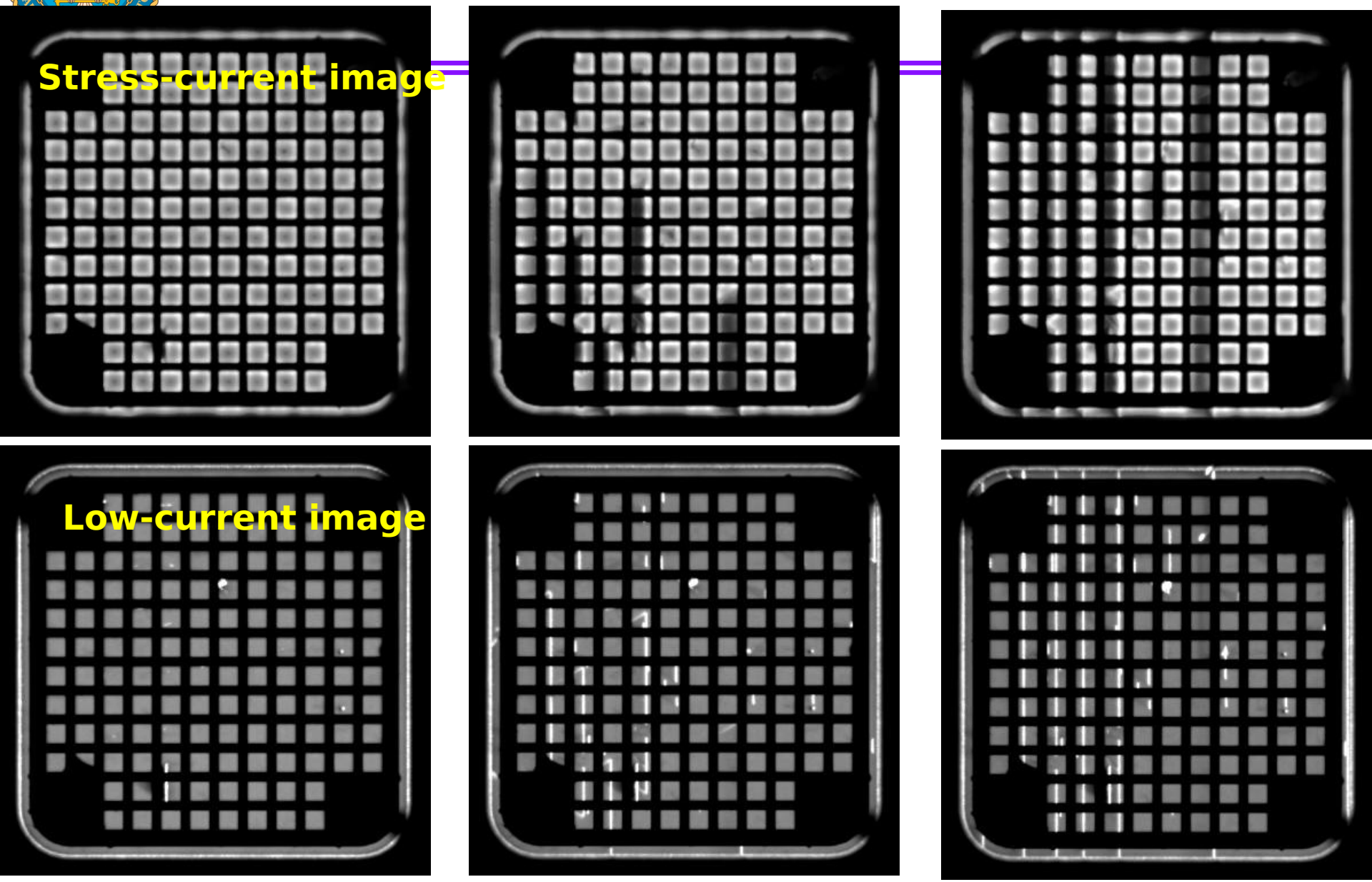
40 x 40 µm openings in anode metal allow light emission images to be collected

Emission Image

Top View

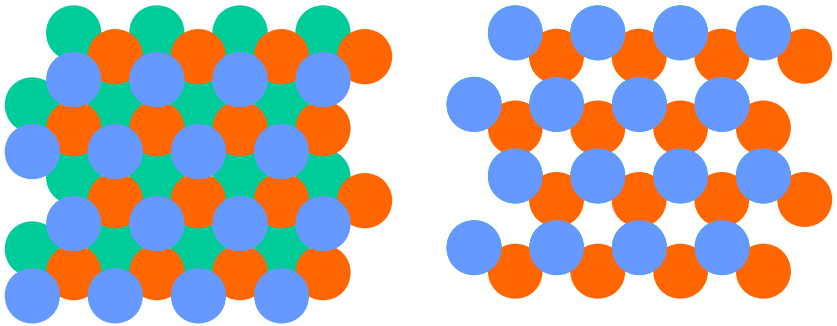
Stacking Fault Growth at 1 A (160 A/cm²)

4.26 V pre-stress | 4.30 V 9 min | 4.54 V 50 min



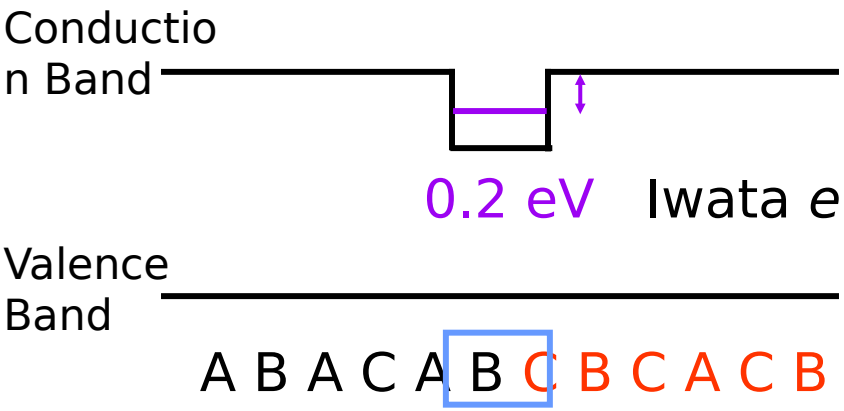
Quantum Well due to a Stacking Fault

Possible Stacking Orders

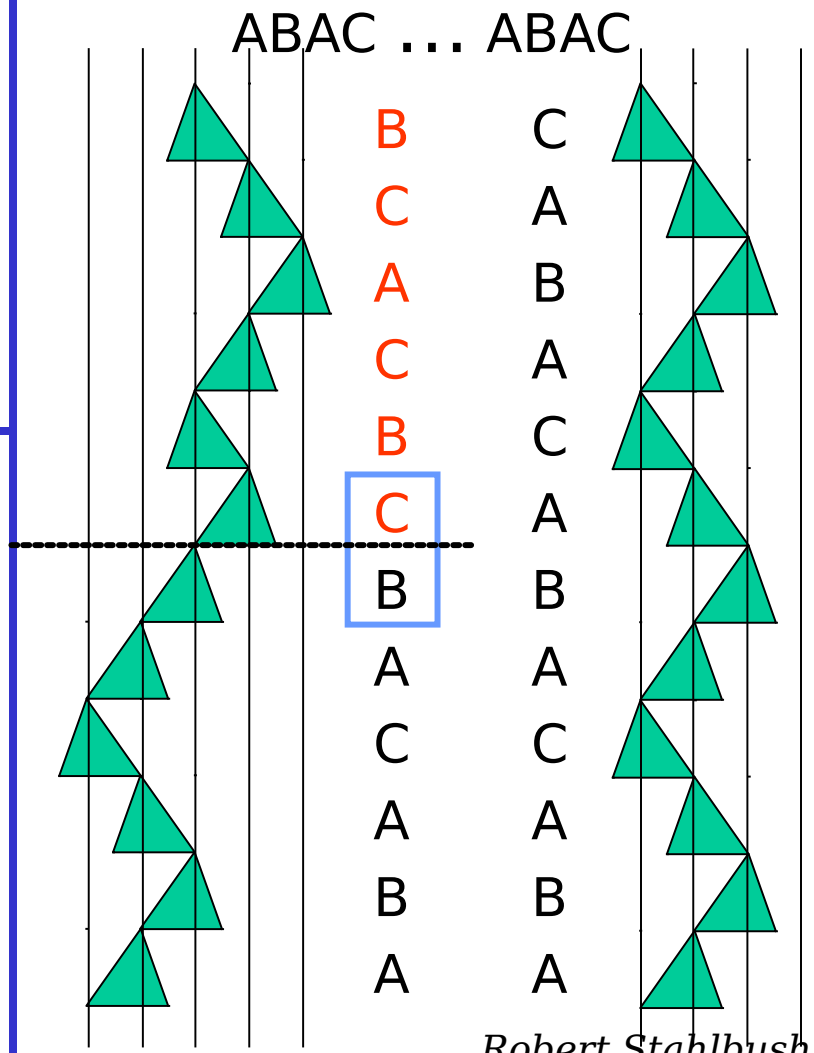


ABC … ABA …

Quantum Well at Stacking Fault

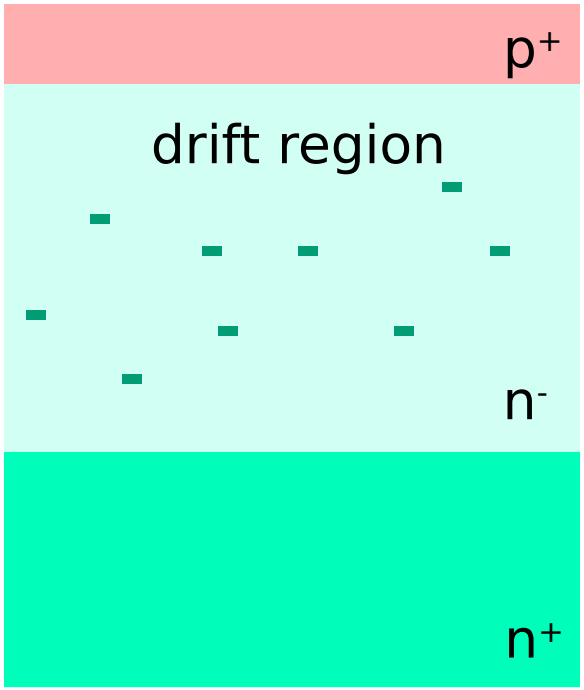


4H Stacking Sequence

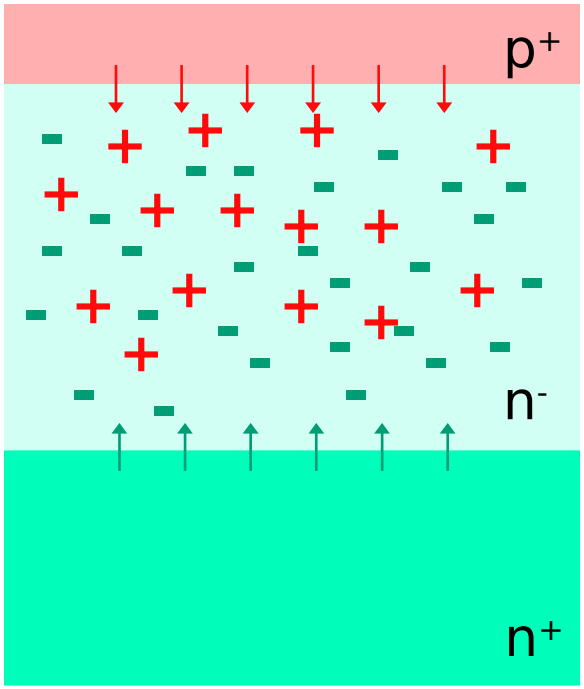


Effect of Stacking Fault in Diode Drift Region Forward Current Reduction

V = 0

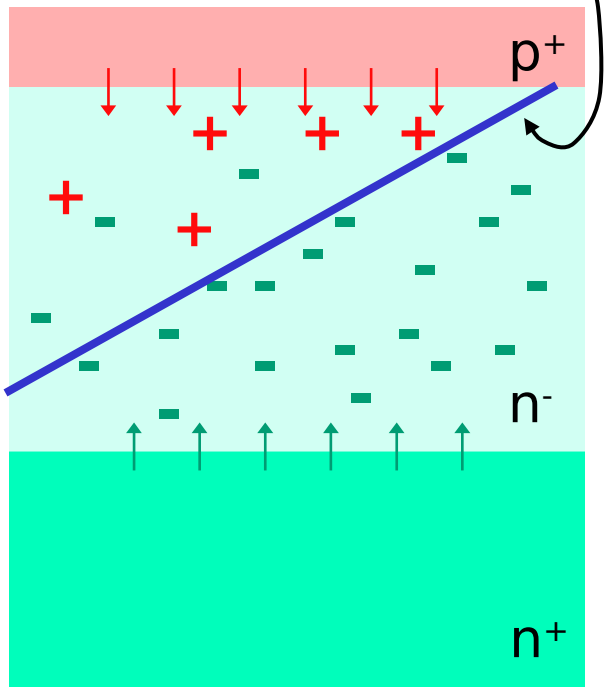


V > 0
high current



both hole and electron concentrations increase

V > 0
with stacking fault



recombination at quantum well reduces lifetime

hole and electron concentrations

Schematic of Light Emission Images

plan view

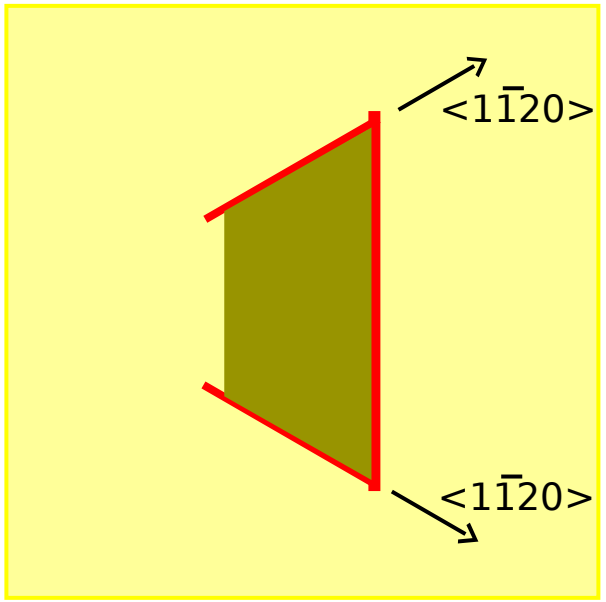
Dark area in Stress-current images

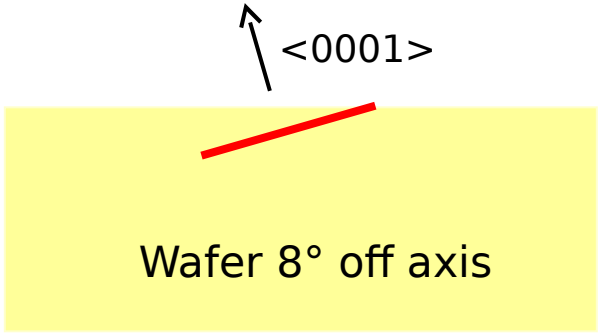
Reduced current flow

Bright lines in low-current images

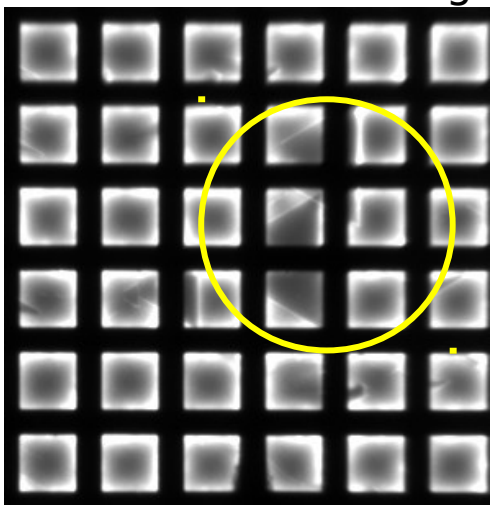
Dislocations

cross-sectional view

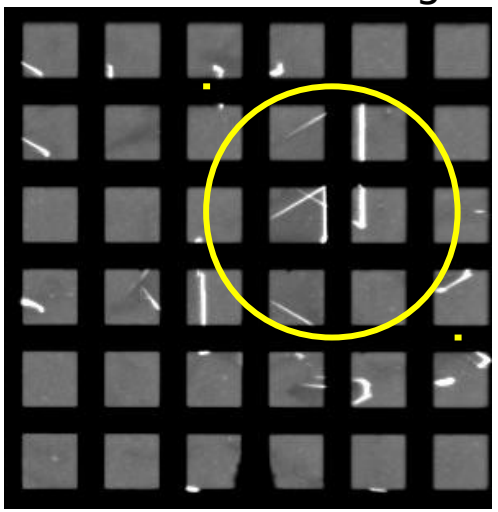




Stress-current image



Low-current image

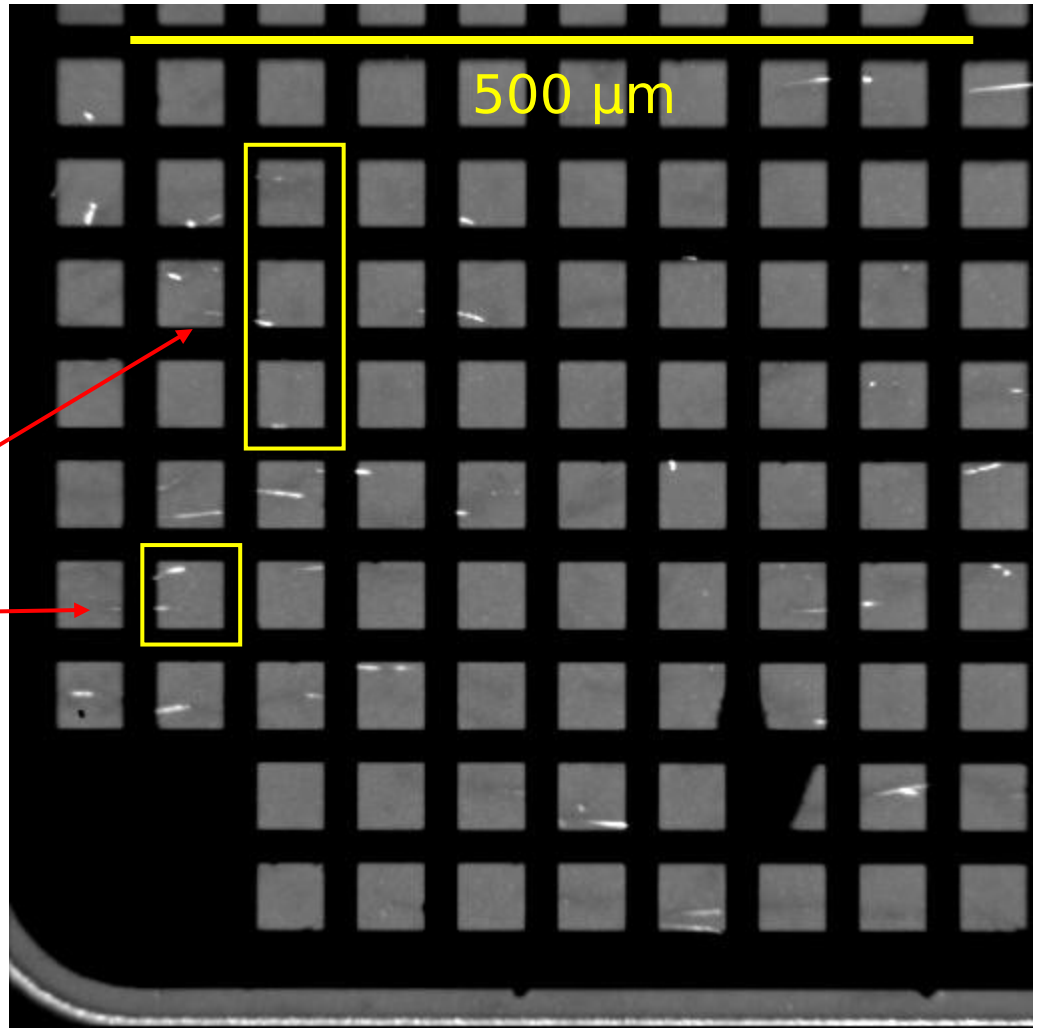


Pre-Stress Light Emission Image of PiN Diode

Dark grid is the metal covering the anode.

Nucleation Sites ?

Basal Plane Dislocations

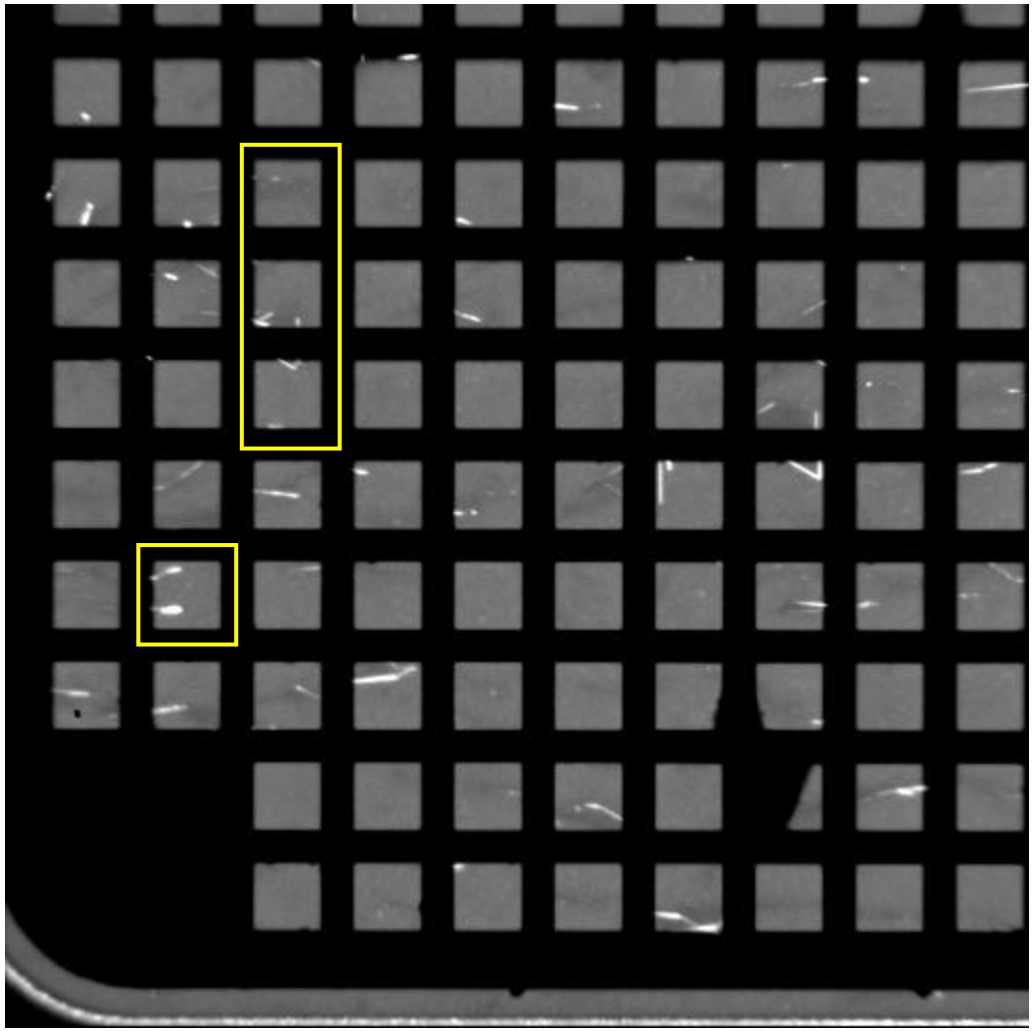


Stacking Faults Nucleation in Epi Layer

<0001>

Wafer 8° off axis

Cross Sectional View

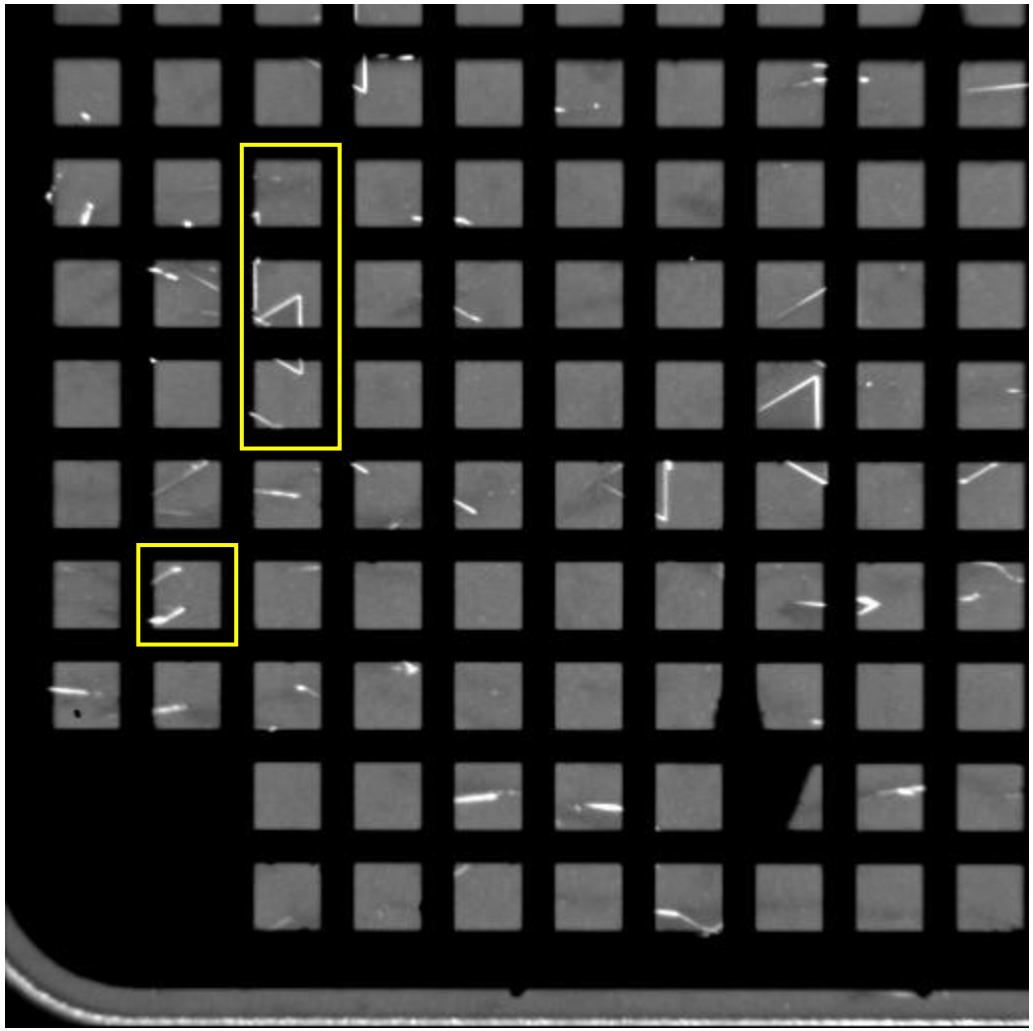


I = 1.0 A

Stacking Faults Nucleation in Epi Layer

<0001>

Wafer 8° off axis

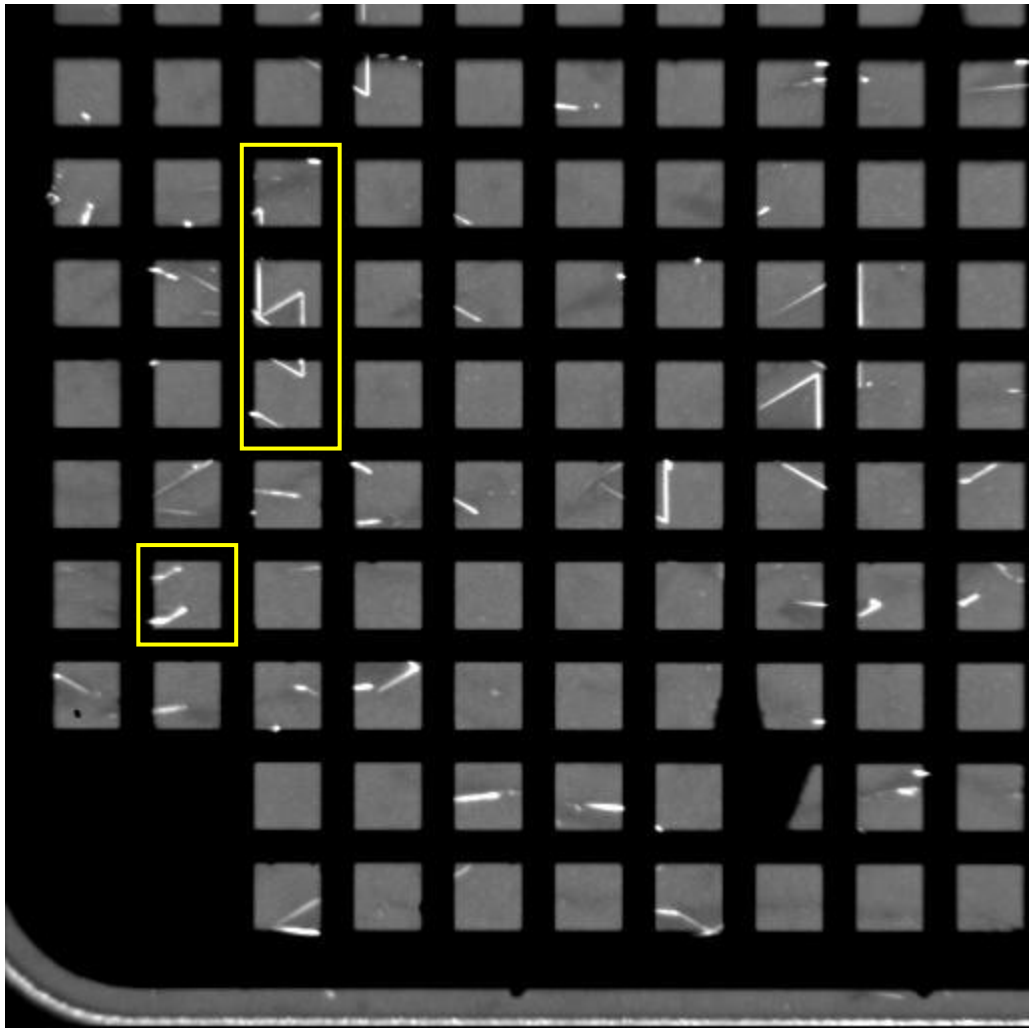


I = 1.0 A

Stacking Faults Nucleation in Epi Layer

<0001>

Wafer 8° off axis

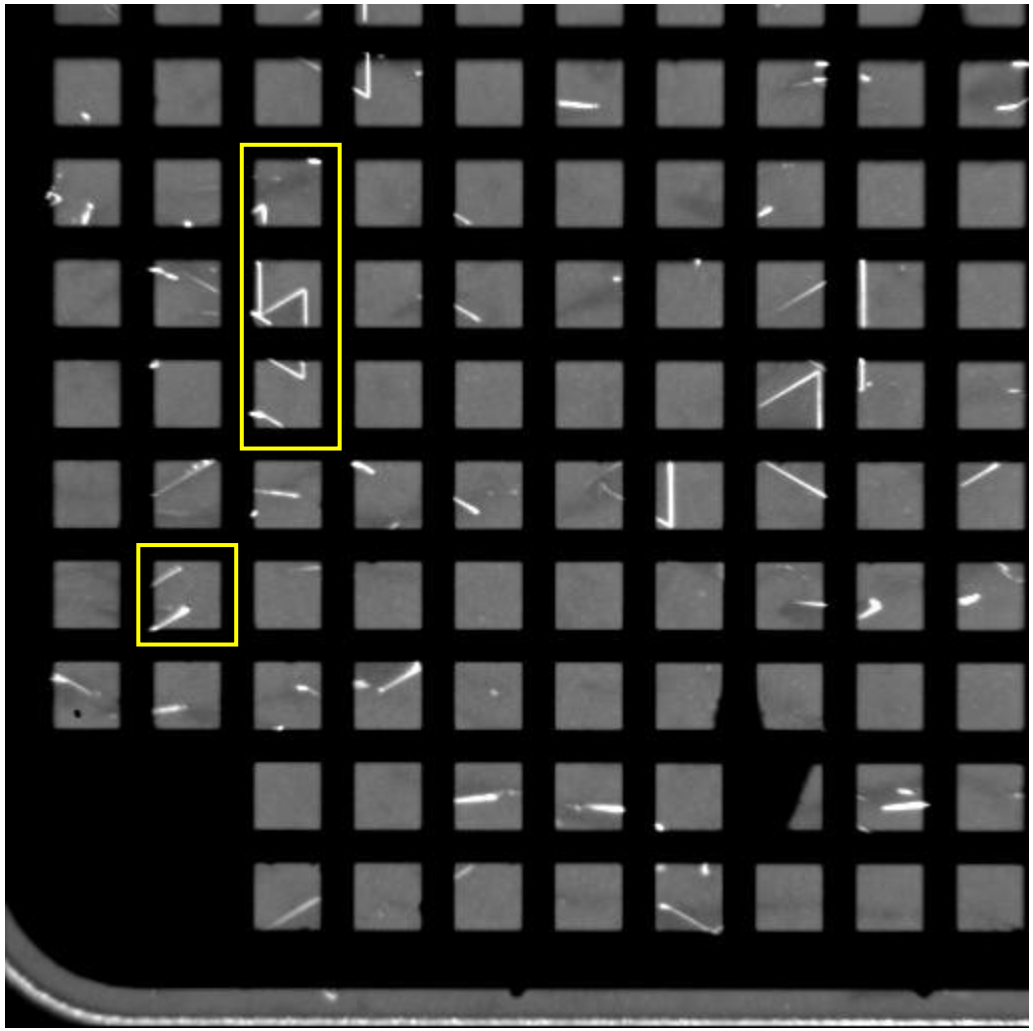


I = 1.0 A

Stacking Faults Nucleation in Epi Layer

<0001>

Wafer 8° off axis

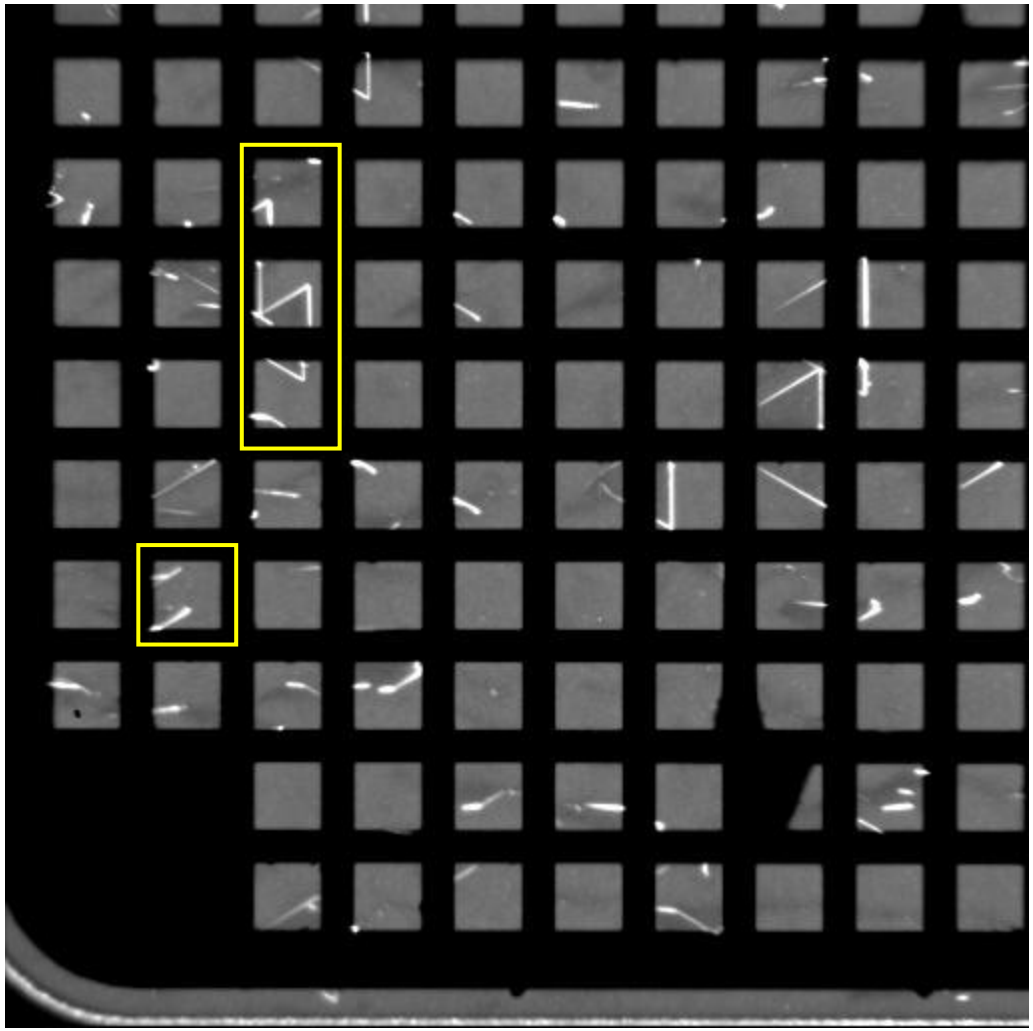


I = 1.0 A

Stacking Faults Nucleation in Epi Layer

<0001>

Wafer 8° off axis

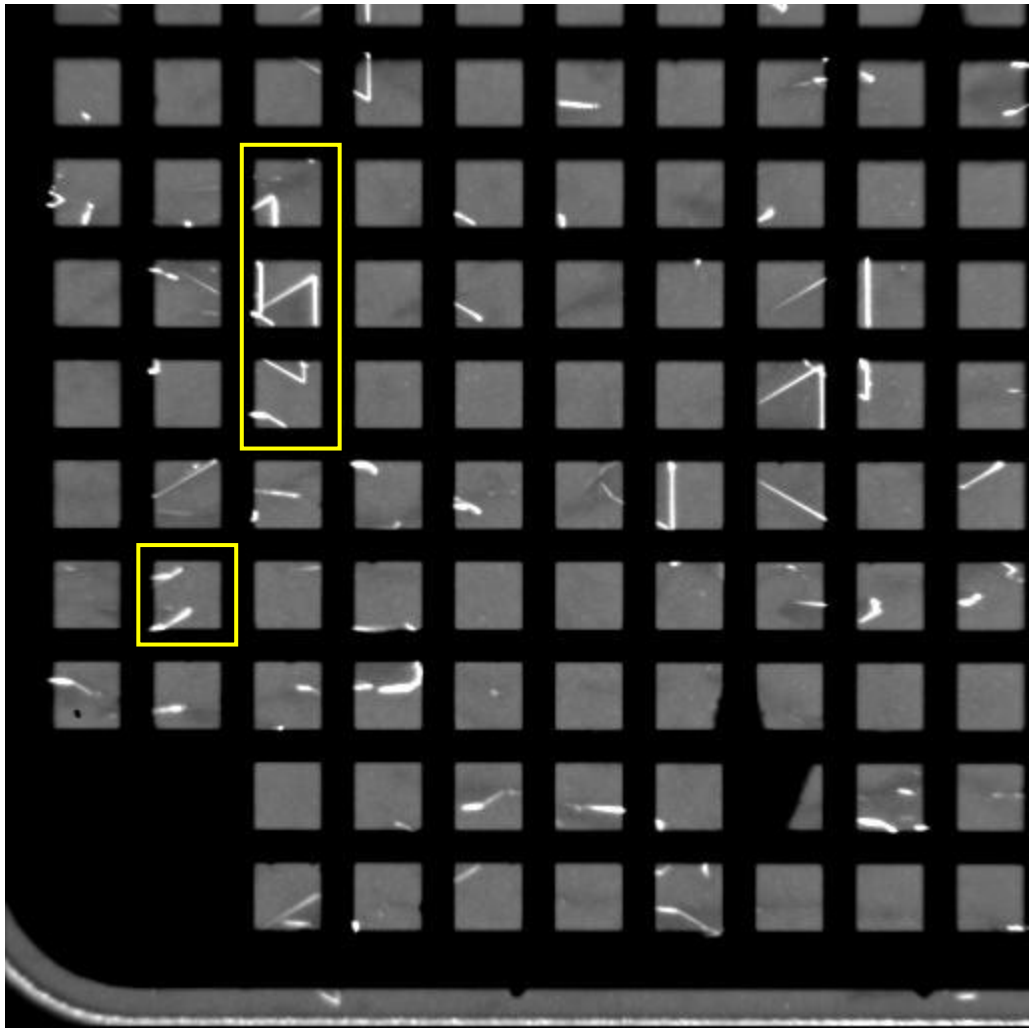


I = 1.0 A

Stacking Faults Nucleation in Epi Layer

<0001>

Wafer 8° off axis

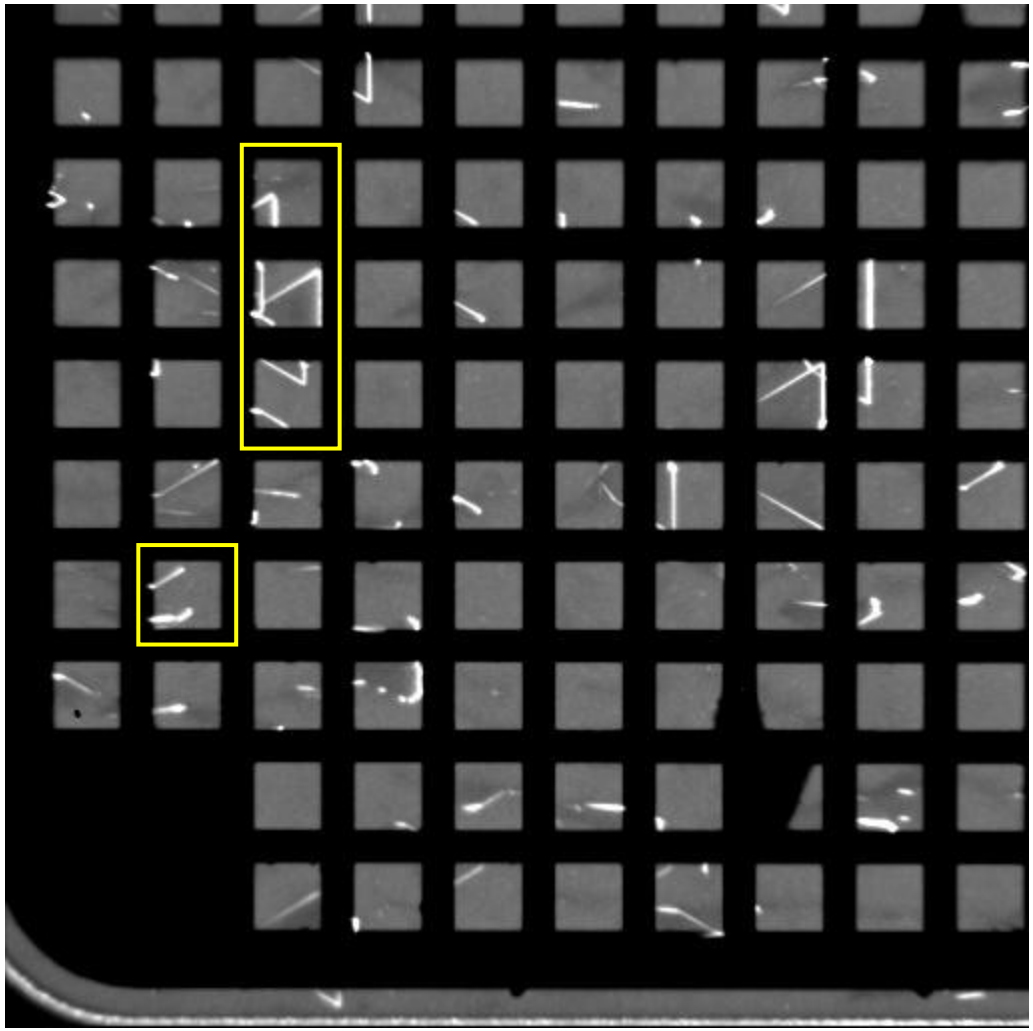


I = 1.0 A

Stacking Faults Nucleation in Epi Layer

<0001>

Wafer 8° off axis

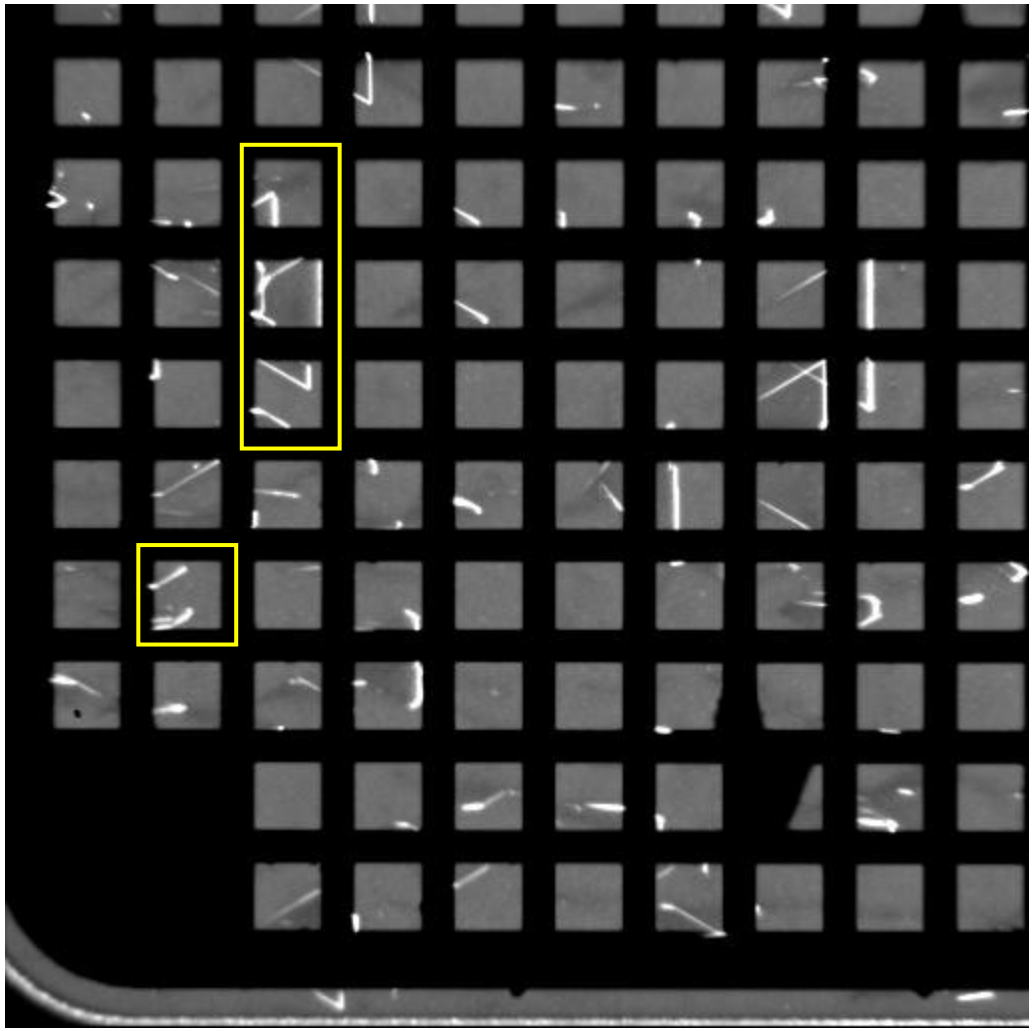


I = 1.0 A

Stacking Faults Nucleation in Epi Layer

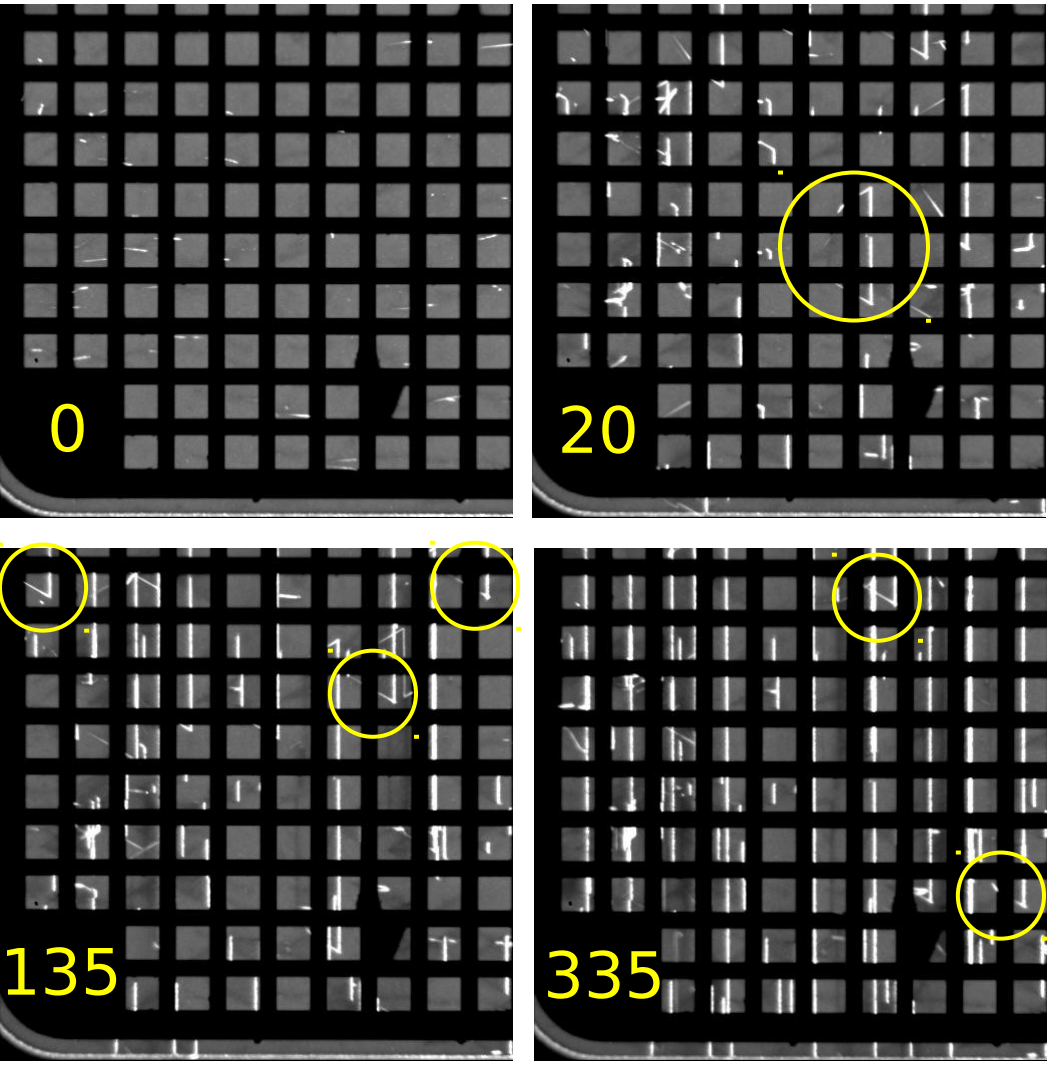
<0001>

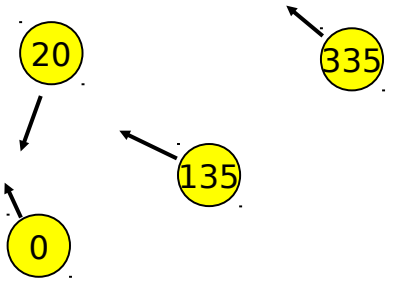
Wafer 8° off axis

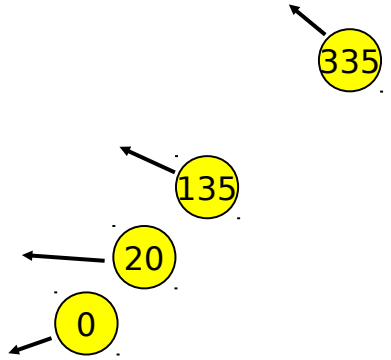


I = 1.0 A

Forward Voltage and Stacking Fault Area

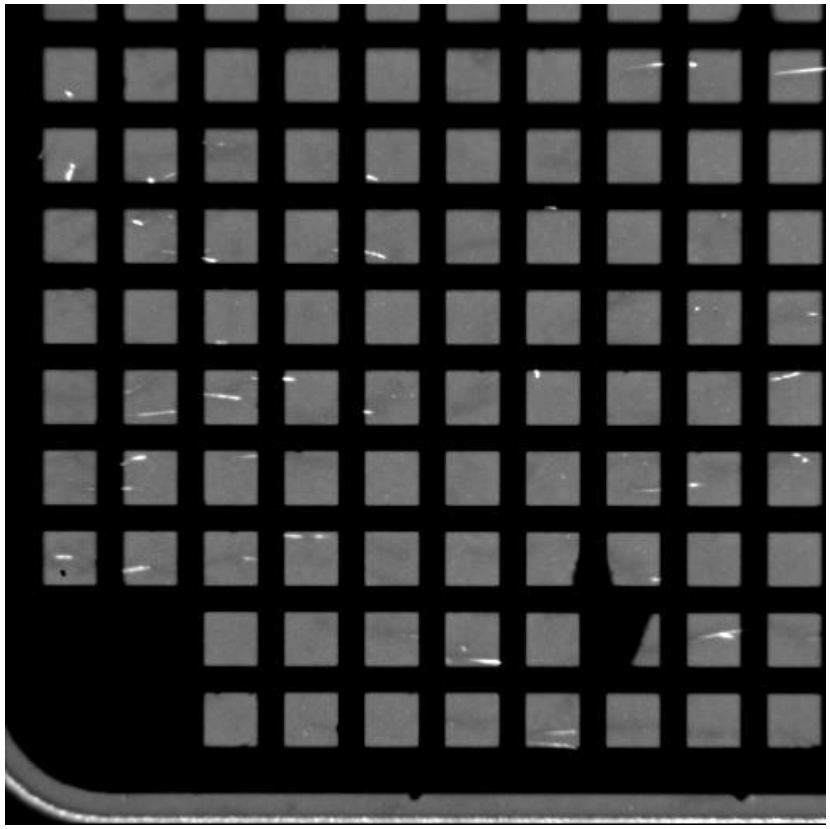




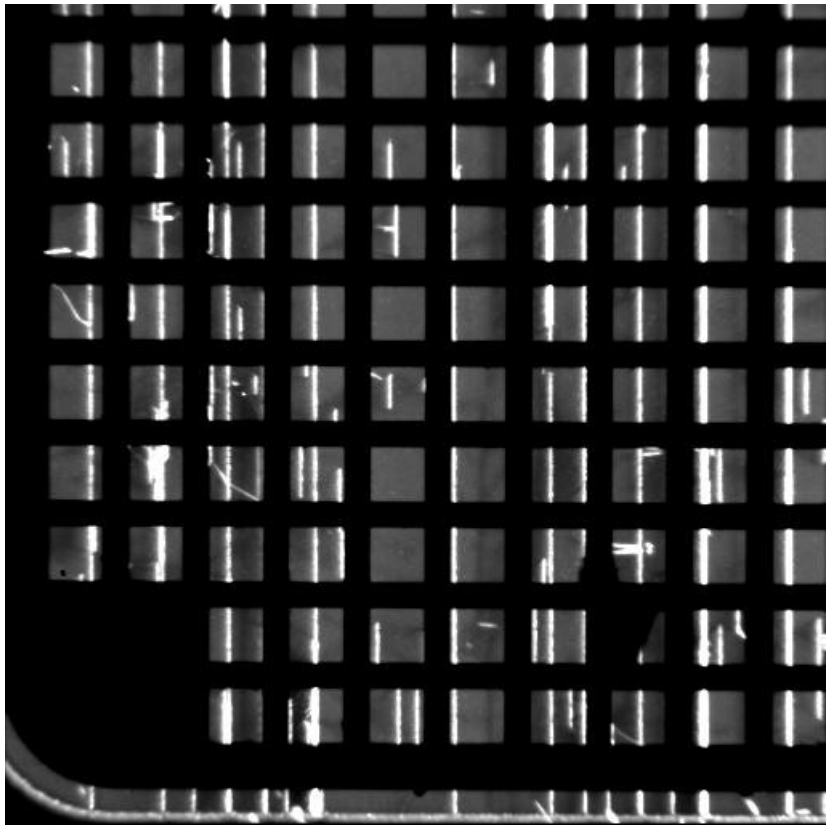


Low Current Images
Before and After Current Stressing
50 min at 160 A/cm^2

4.2 V @ 1.0 A

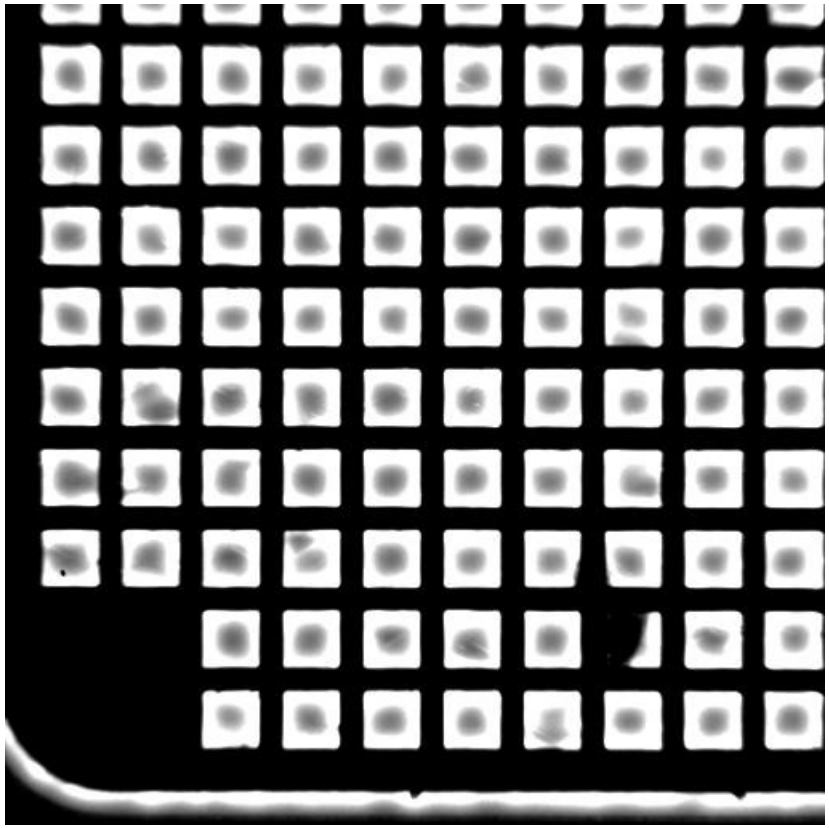


5.1 V @ 1.0 A

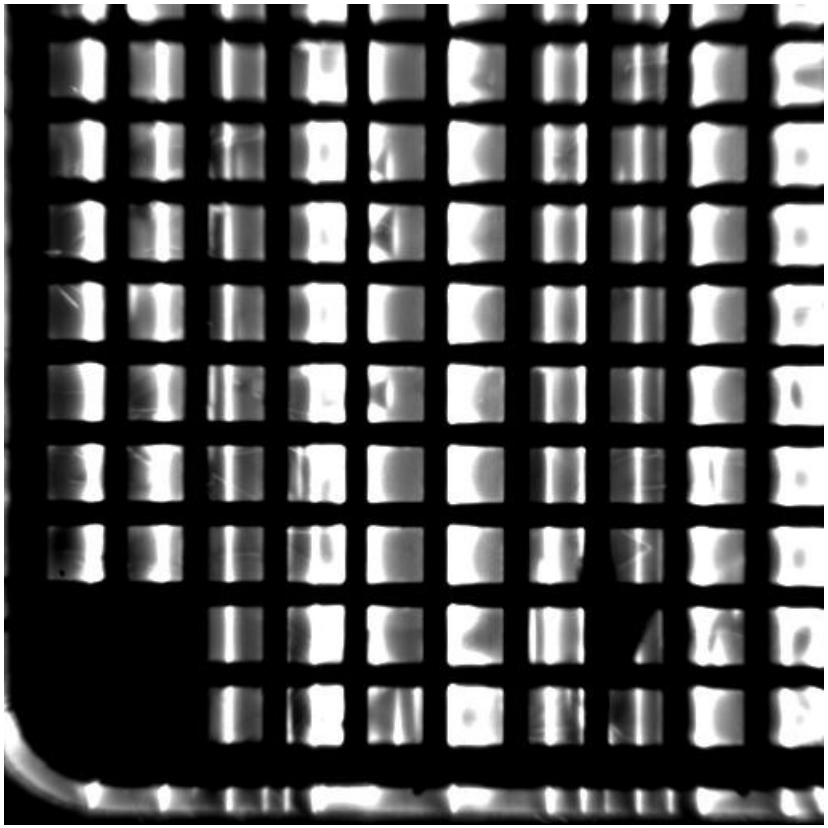


Images at 1.0 A
Before and After Current Stressing
50 min at 160 A/cm²

4.2 V @ 1.0 A



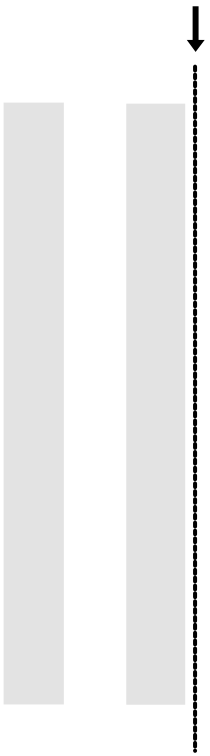
5.1 V @ 1.0 A



Lower current capacity in dark area

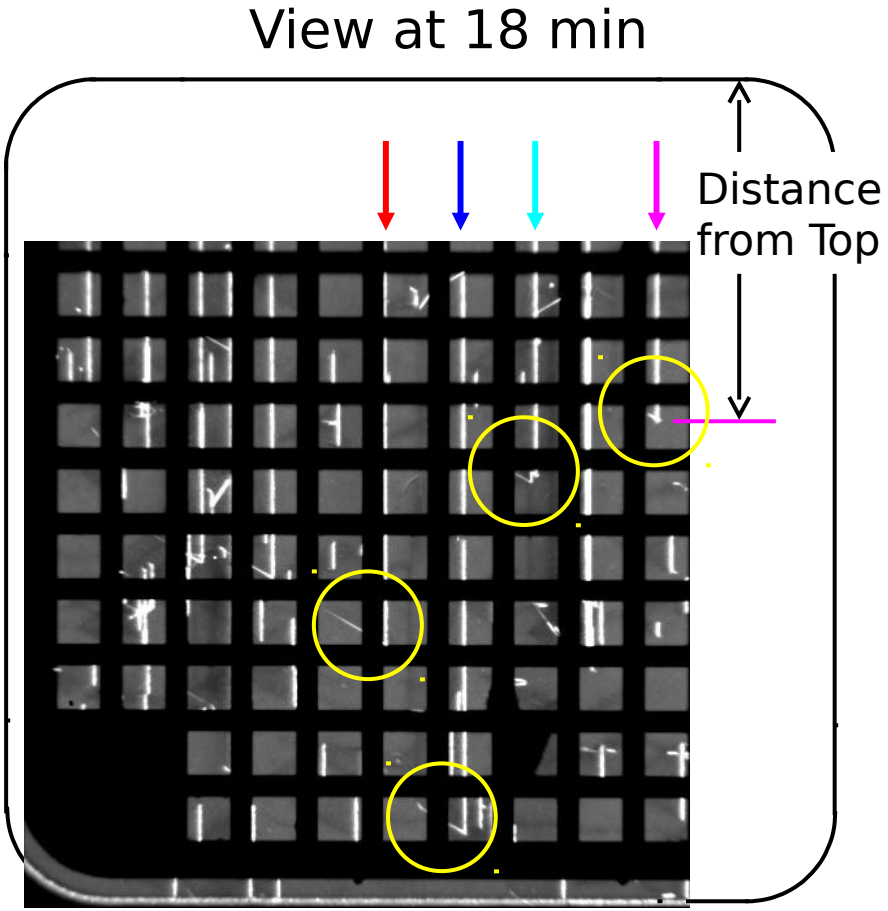
Complicated Role of Mechanical Stress

Growth of Individual Stacking Faults



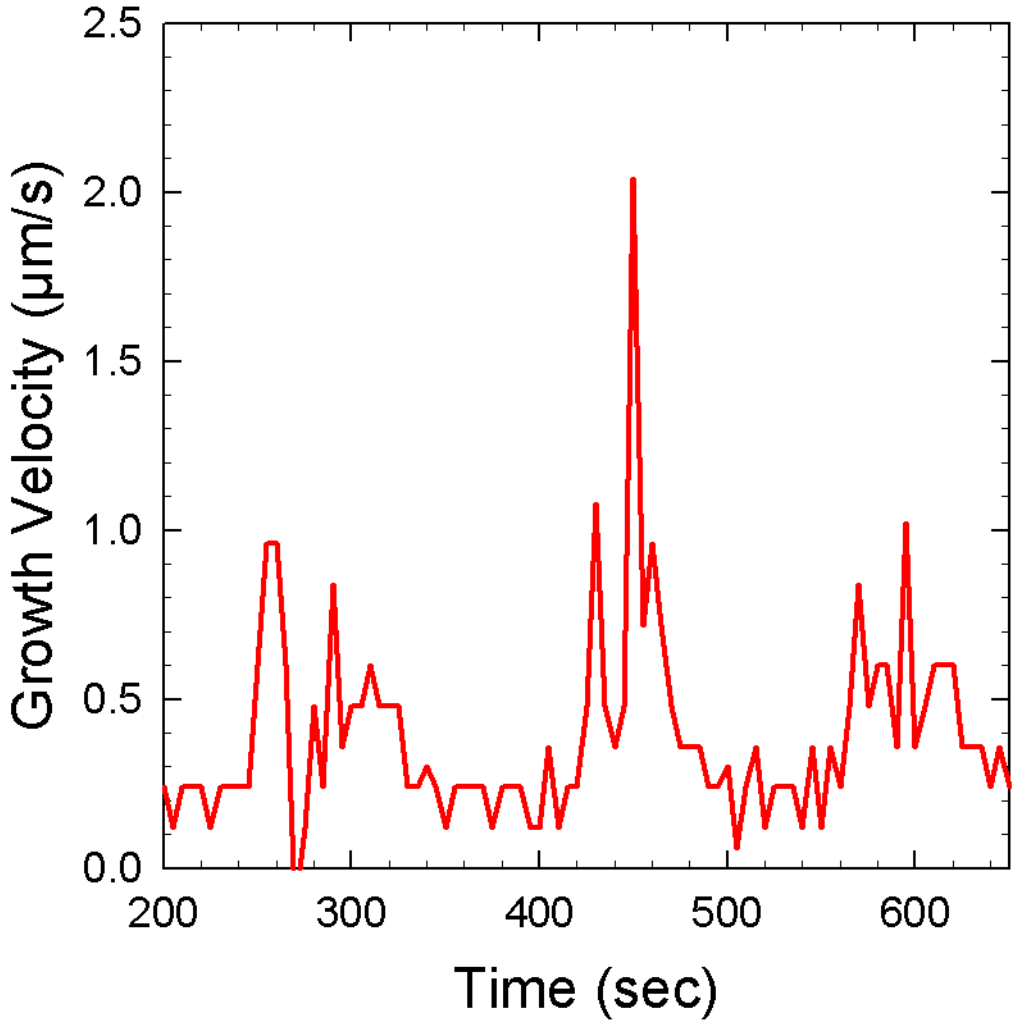
160 A/cm^2

(80 A/cm^2 gray area)



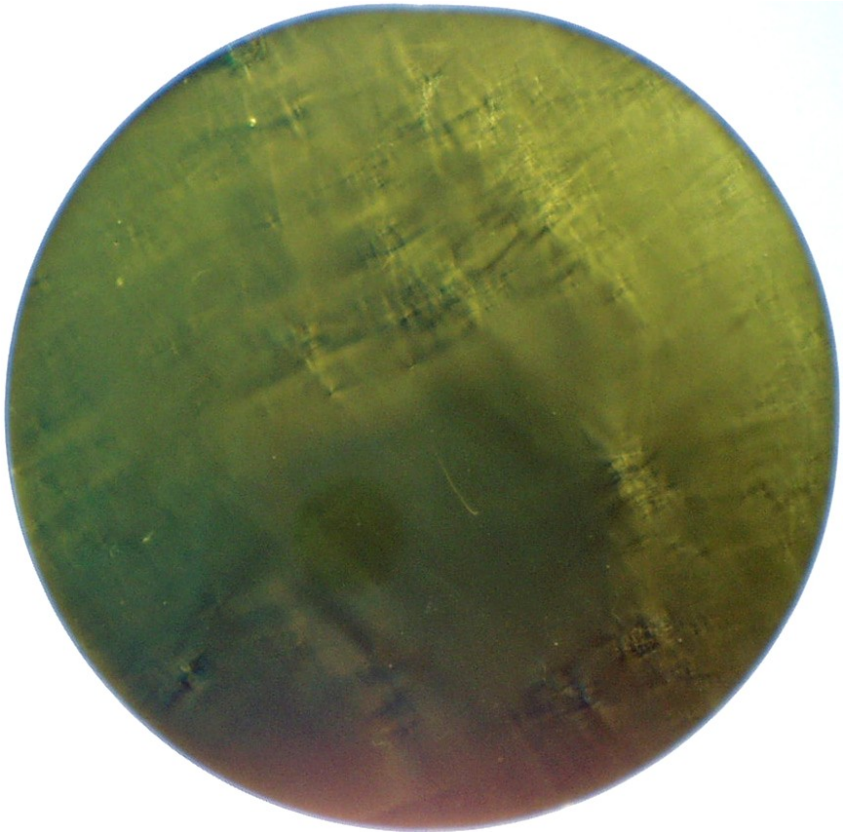
Erratic Stacking Fault Growth Rate

Variations in Local Mechanical Stress

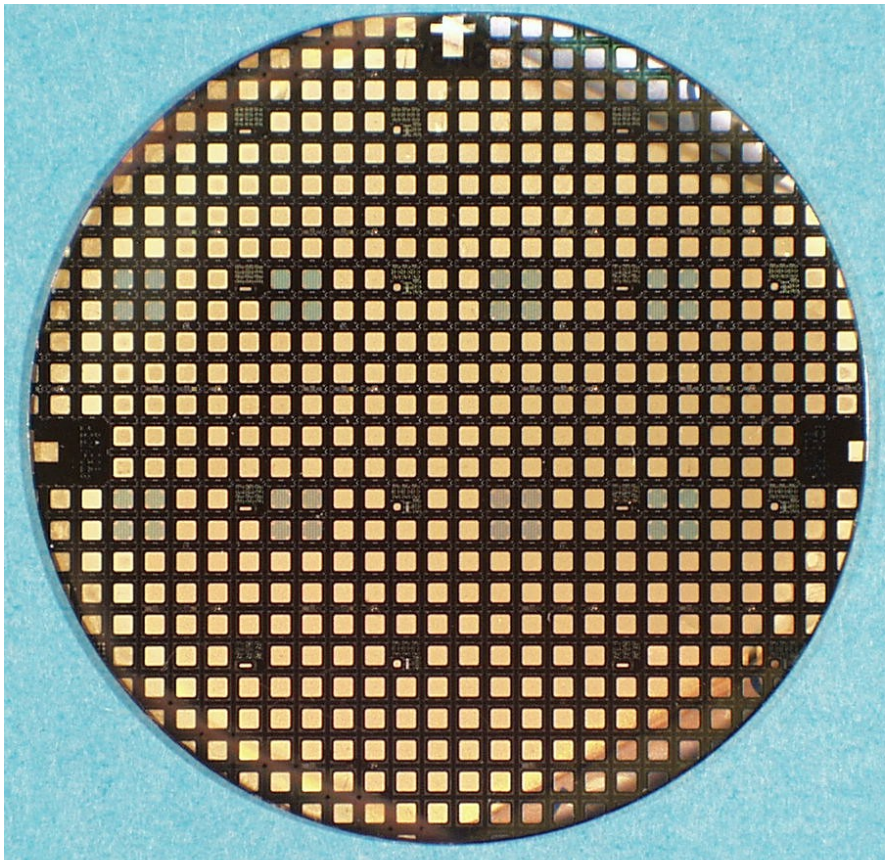


Comparing Stain and Electrical Wafer Maps

Strain Imaged by Crossed Polarizers



Wafer after Pin Diode Fabrication



Electrical Wafer Mapping

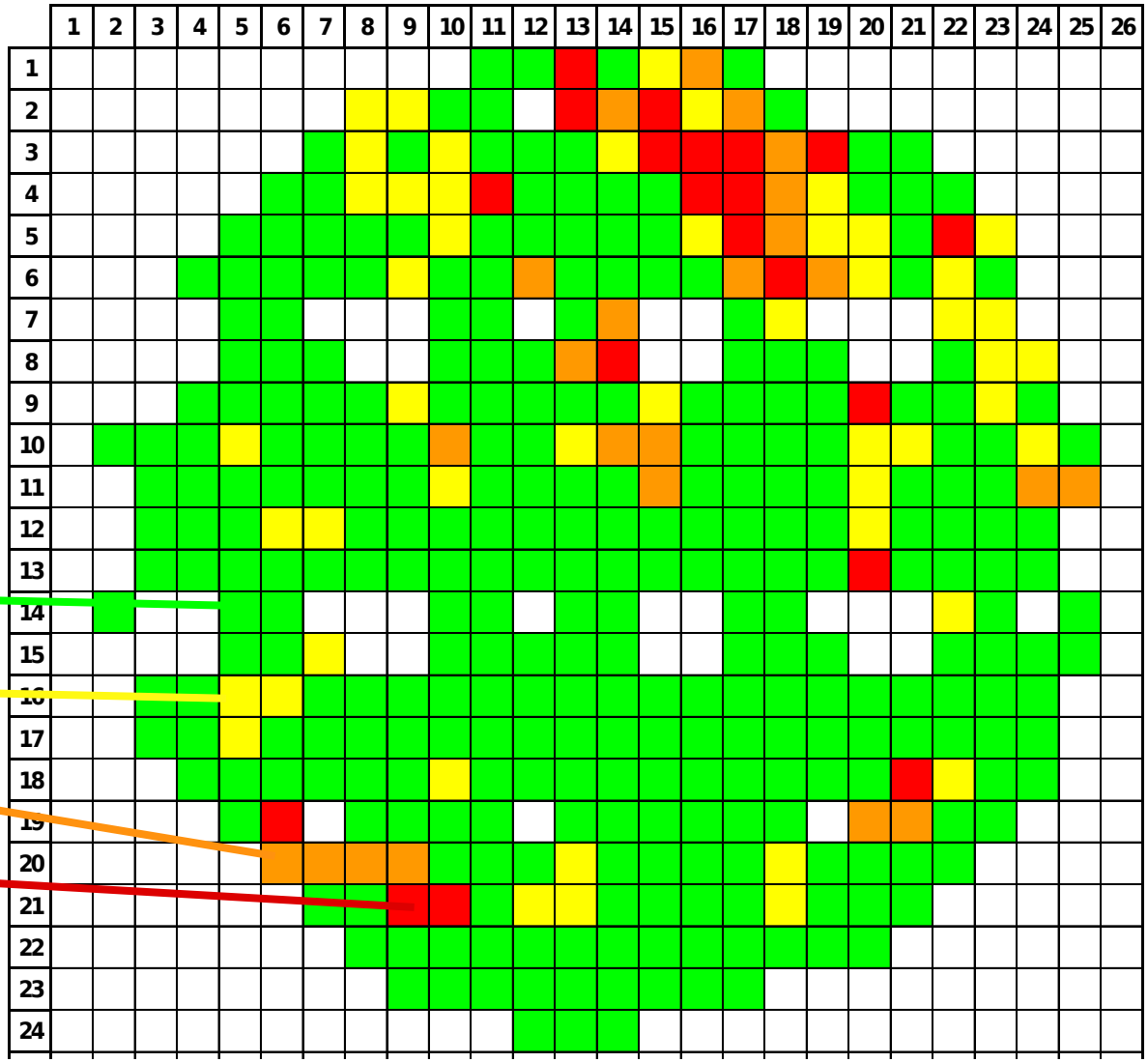
Change in forward voltage after 30 min at 1 A (160 A/cm²)

0 - 0.10 V

0.10 - 0.25 V

0.25 - 0.75 V

0.75 - 1.00 V

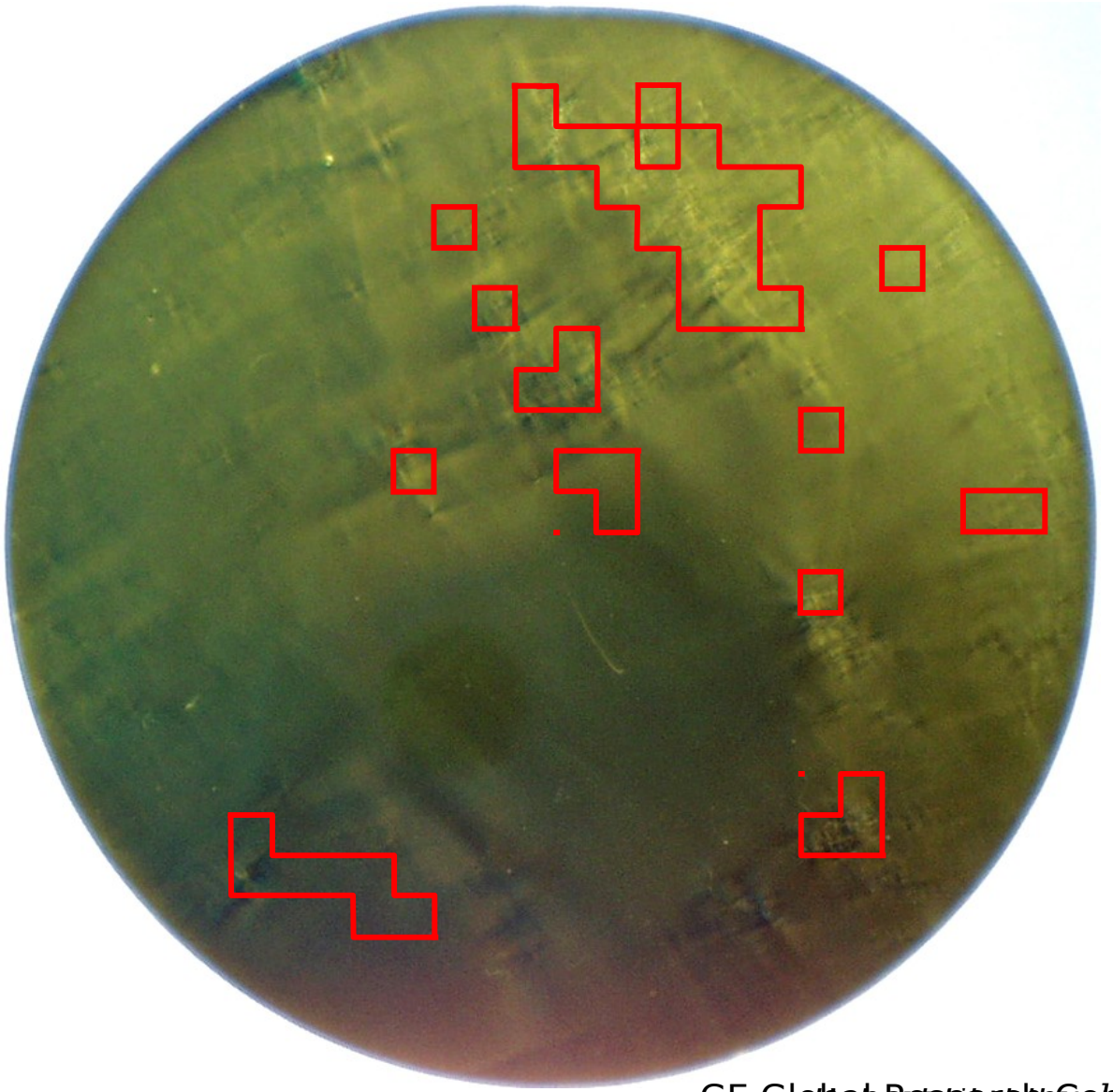


Comparing Stress and Electrical Wafer Maps

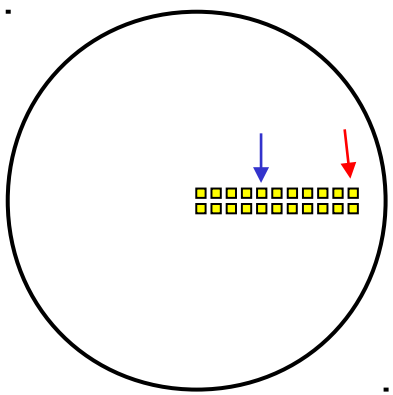
Change in forward voltage after 30 min at 1 A (160 A/cm²)

0.25 - 1.00 V

outlined in red



Stacking Fault Pinning Due to Stress

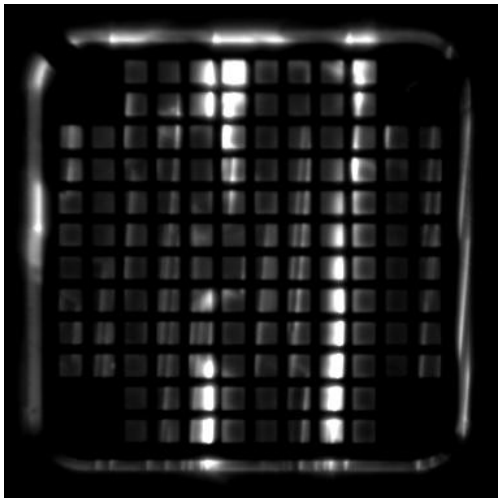


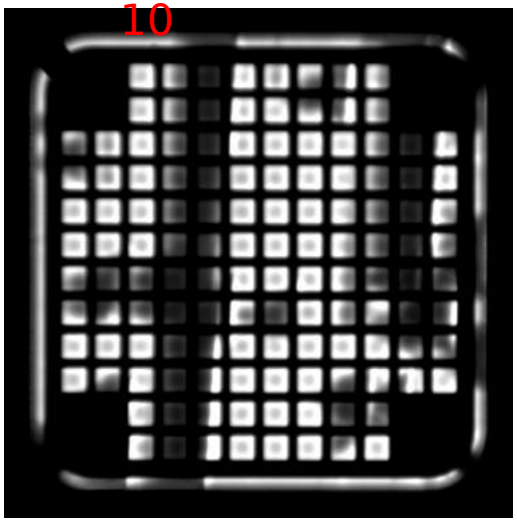
row 0

row 1 column 5

Reliability Problem

row 1 column 10





Center

Edge

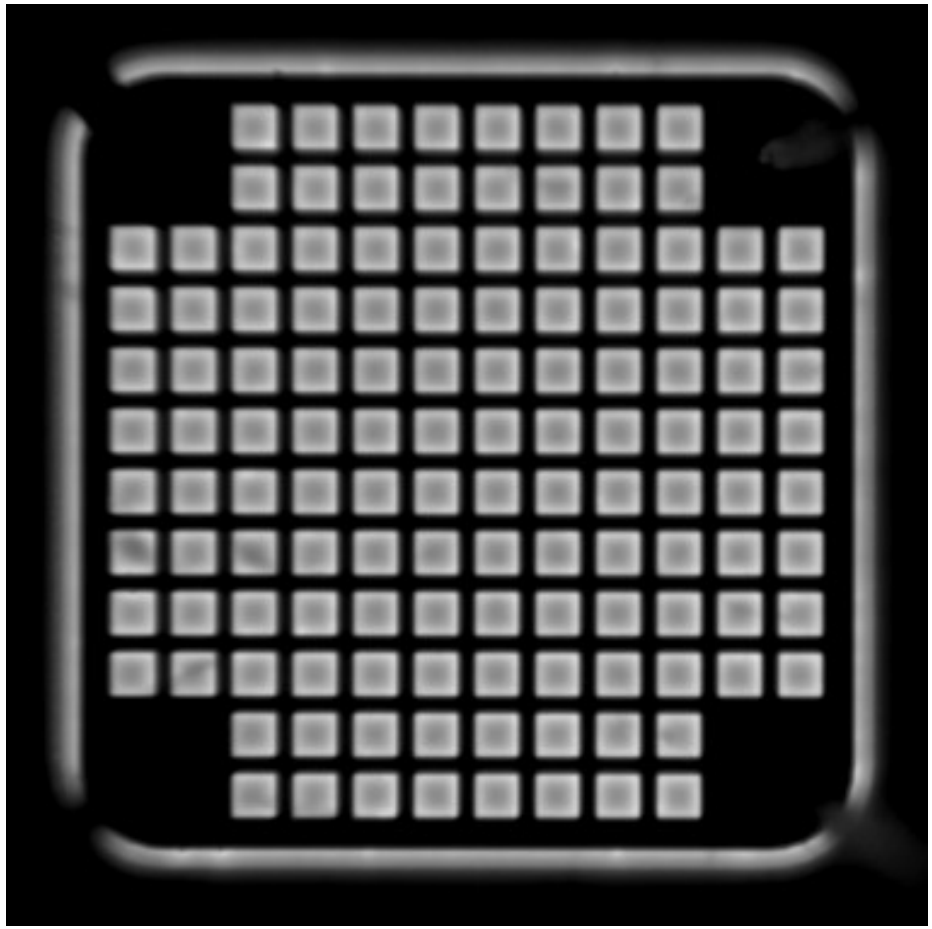
Diode

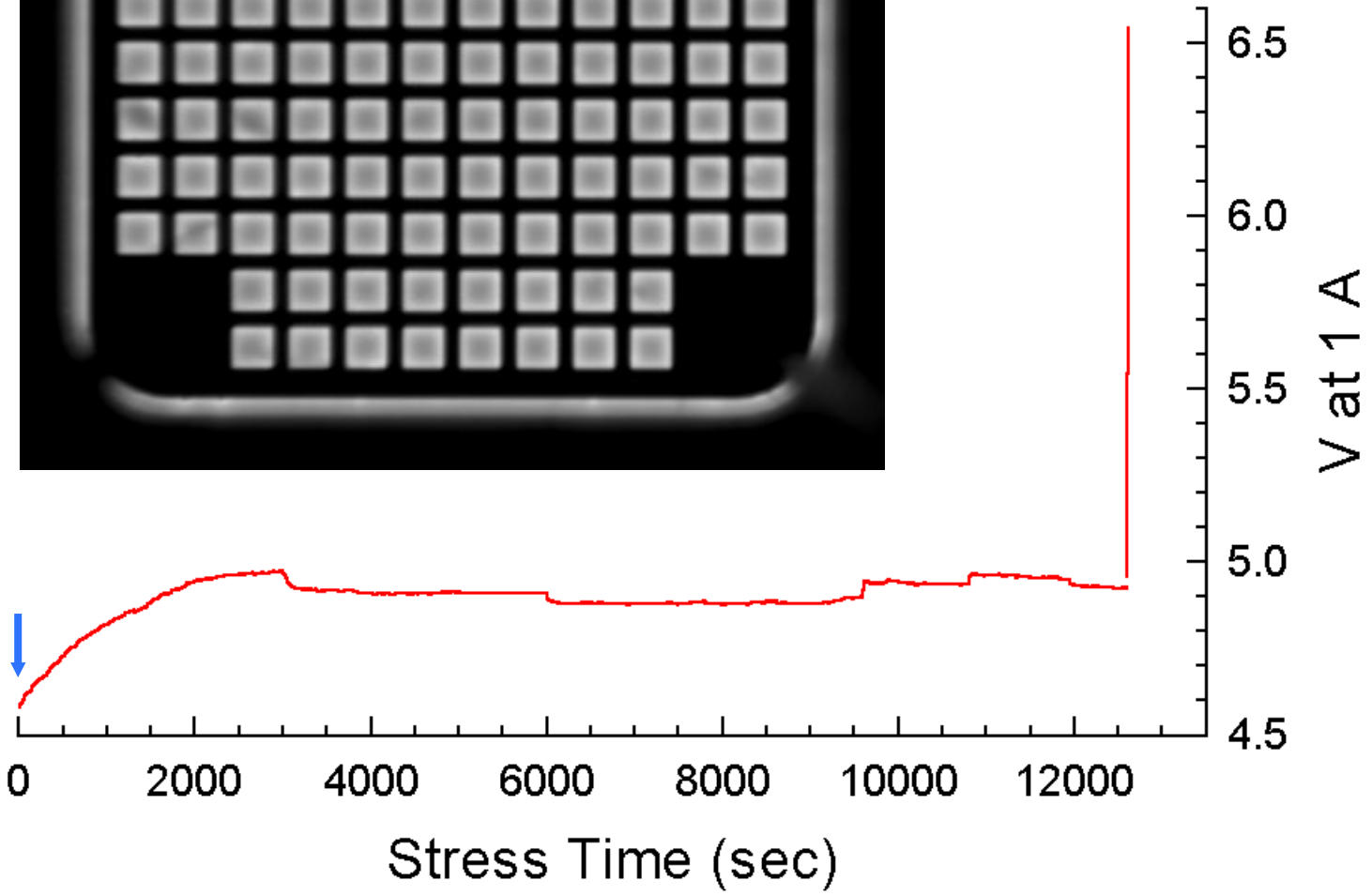
row 1 column 10

Current Stressing

1 A

160 A/cm^2



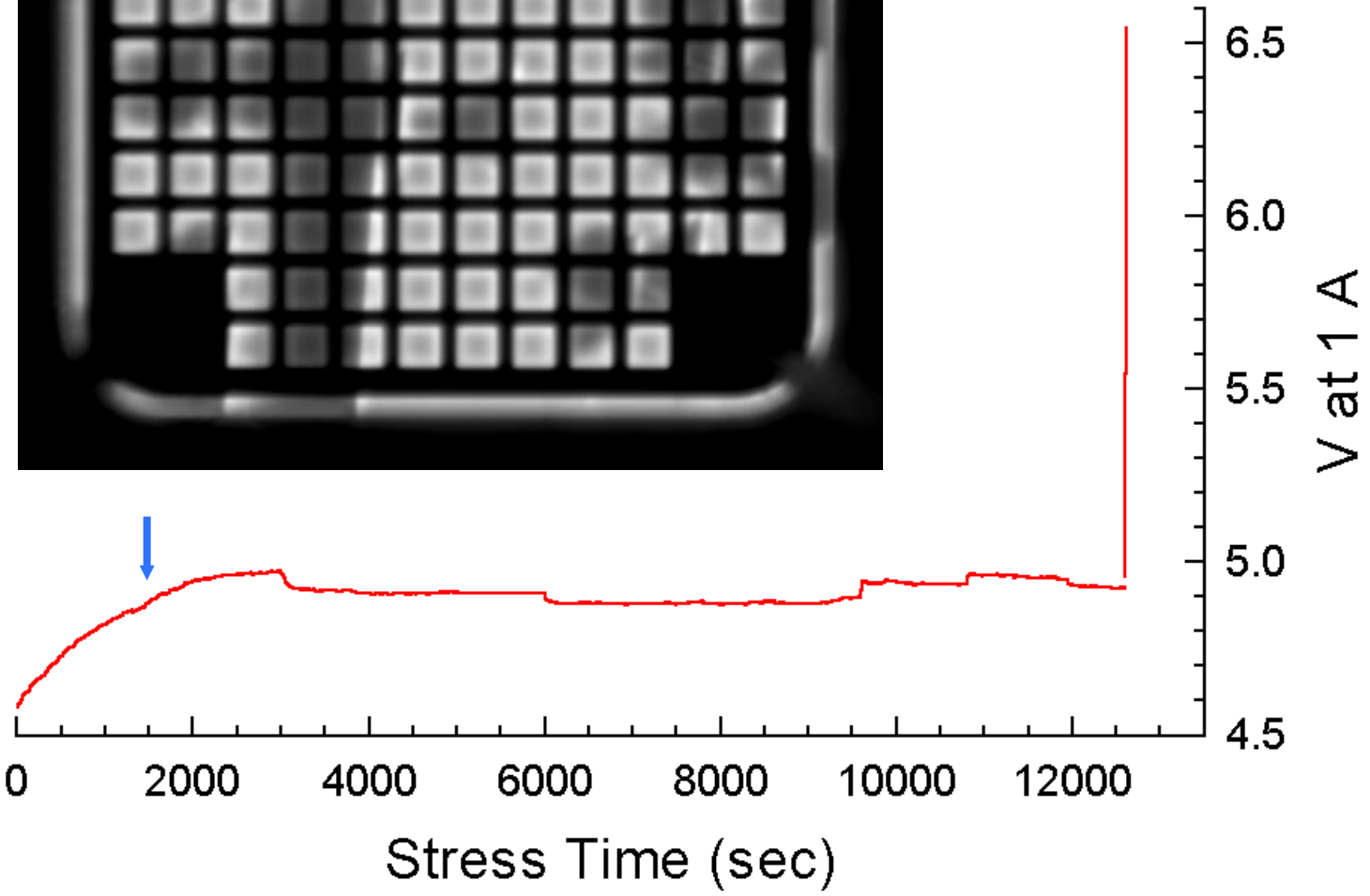


Diode

row 1 column 10

Current Stressing

1 A
160 A/cm^2



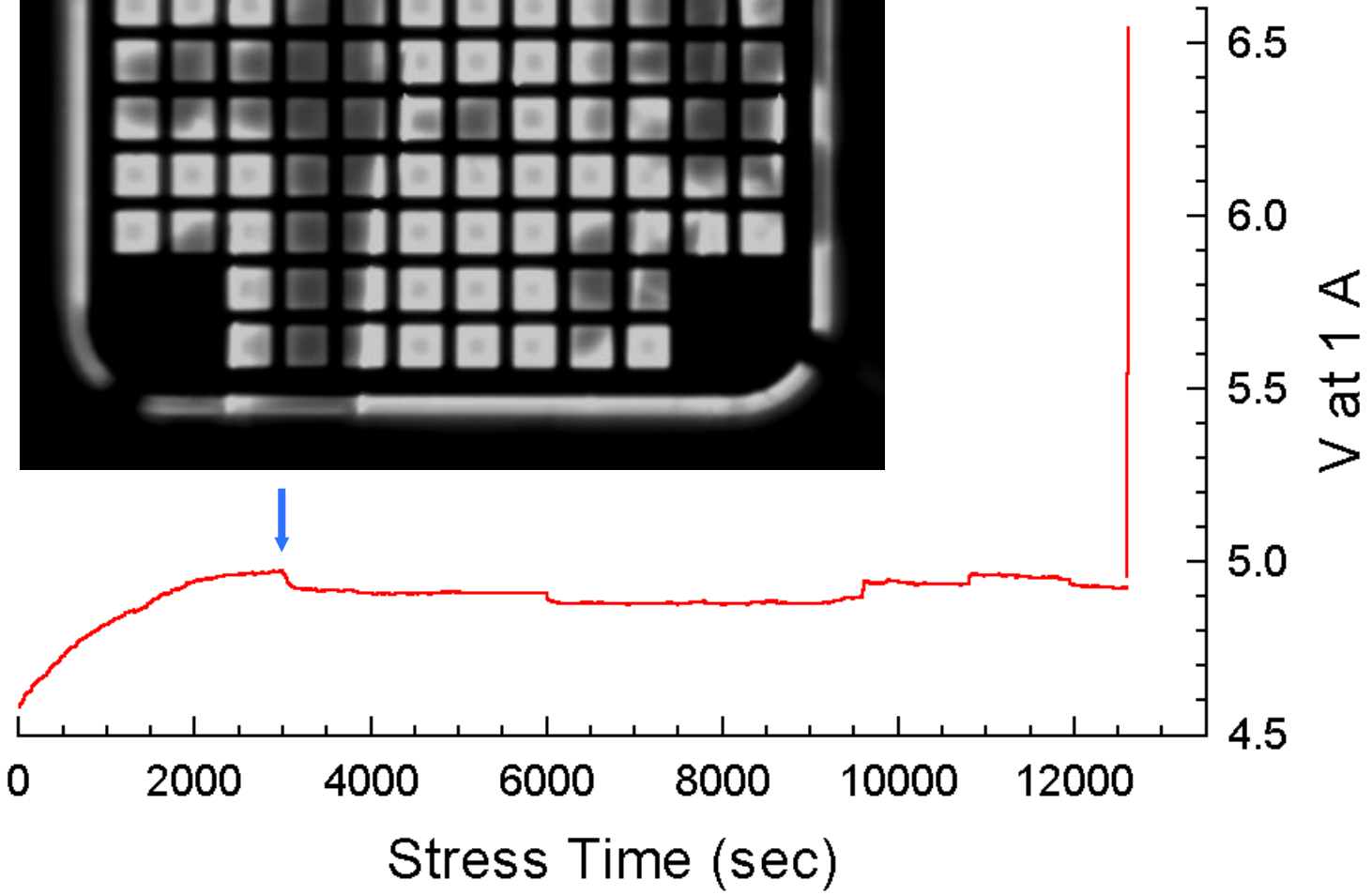
Diode

row 1 column 10

Current Stressing

1 A

160 A/cm^2



205300005

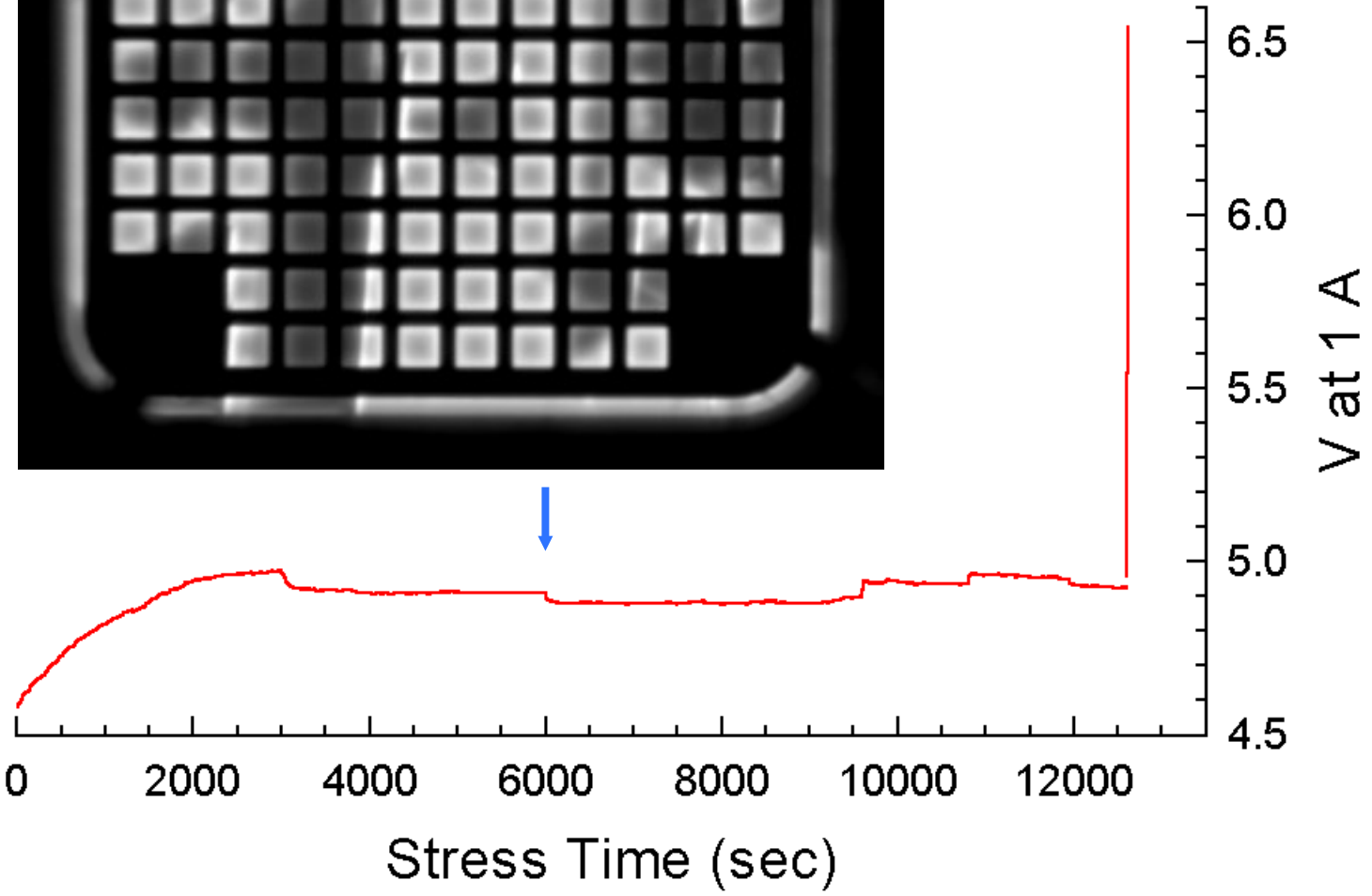
Diode

row 1 column 10

Current Stressing

1 A

160 A/cm^2



205310001

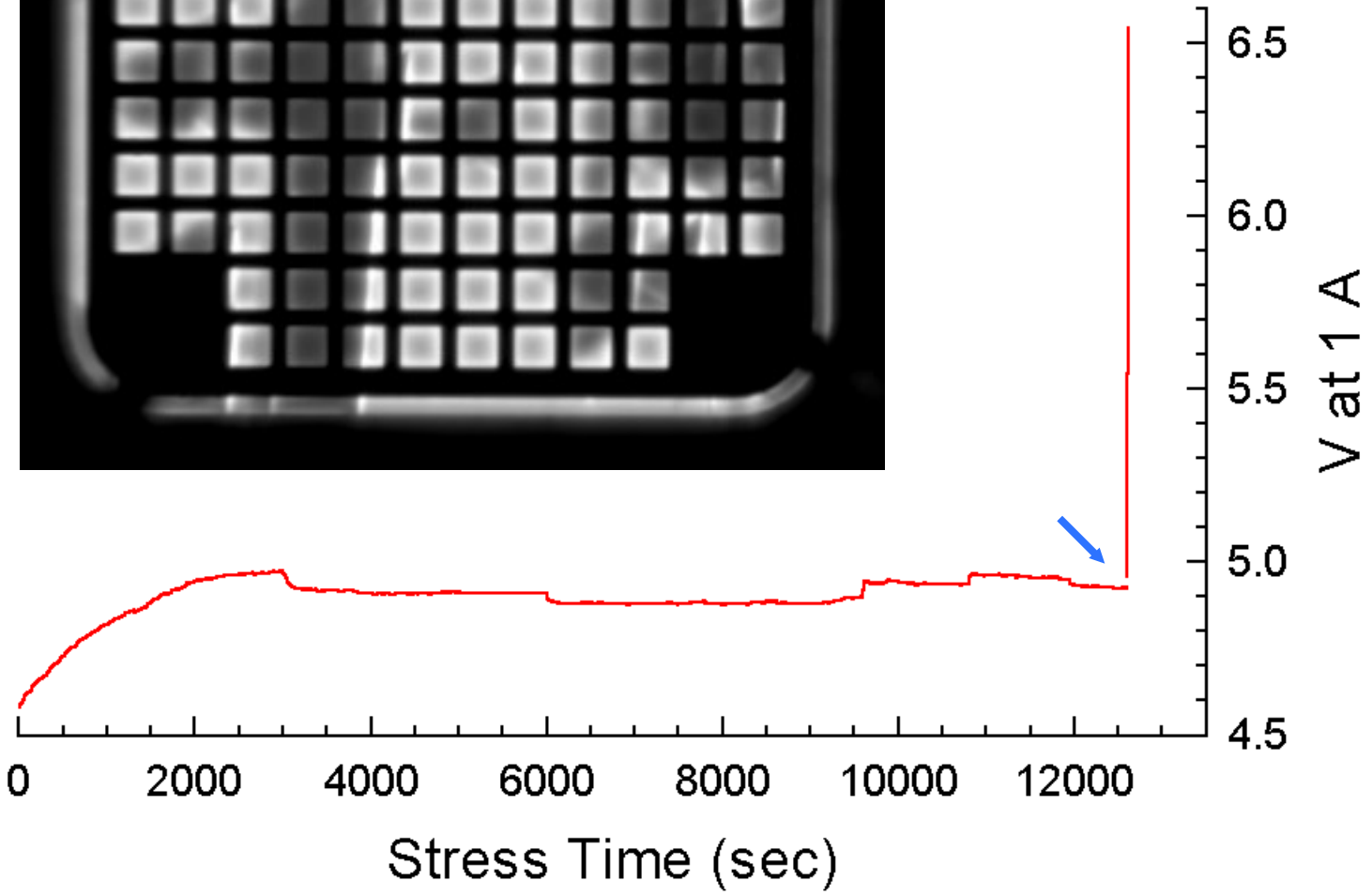
Diode

row 1 column 10

Current Stressing

1 A

160 A/cm^2



206040719

Diode

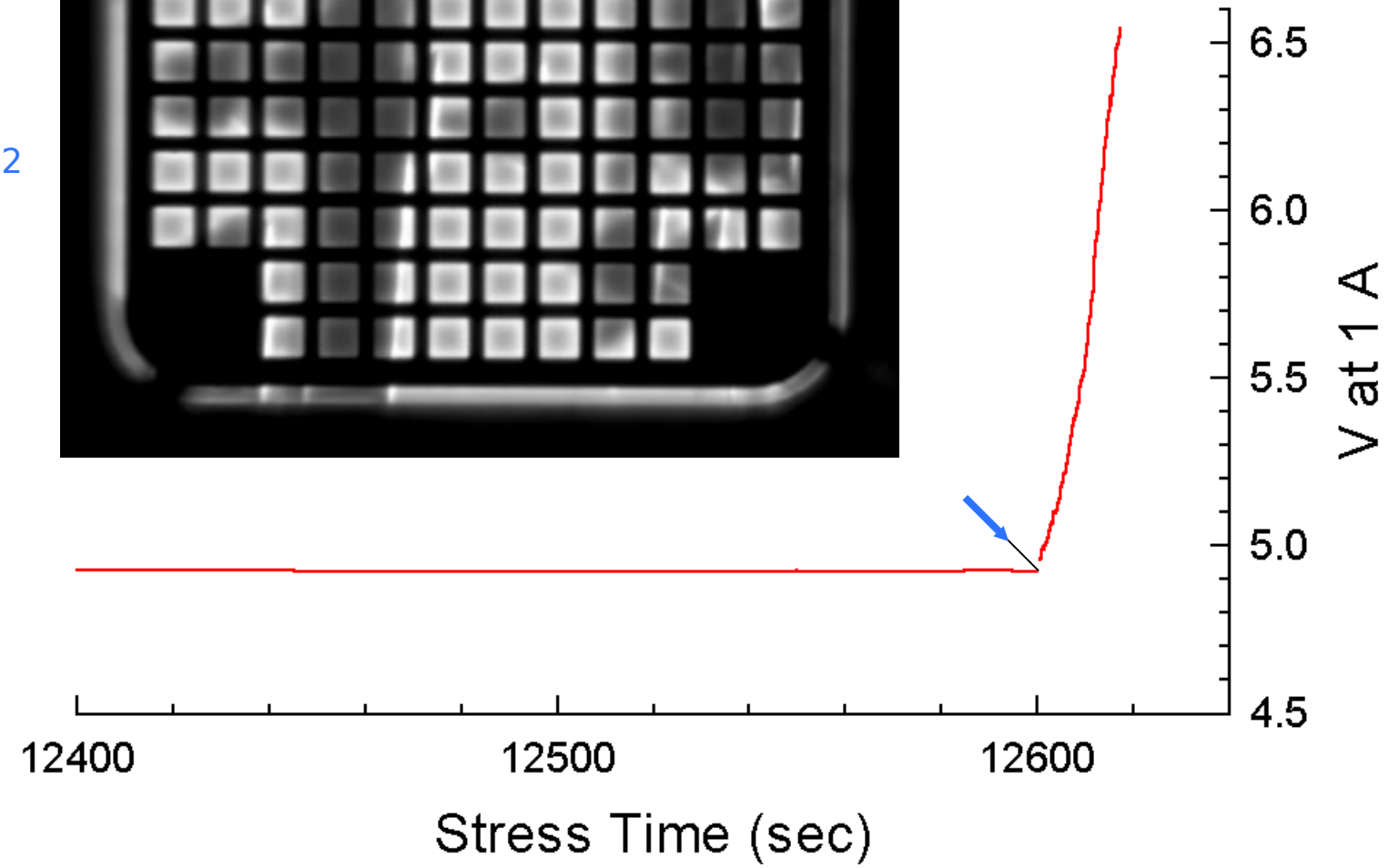
row 1 column 10

Current Stressing

10 A

1600 A/cm²

T<120°C



206040719

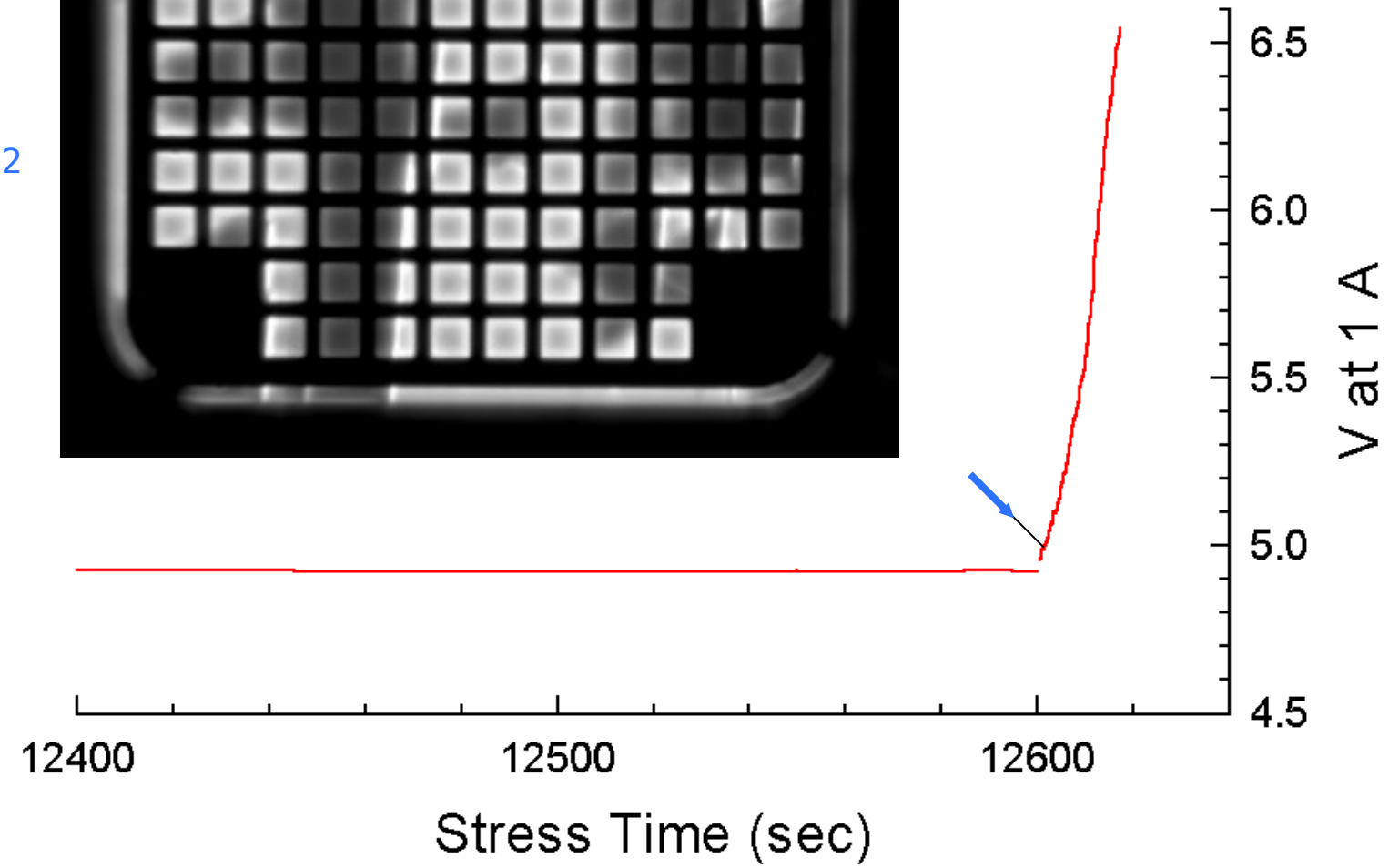
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



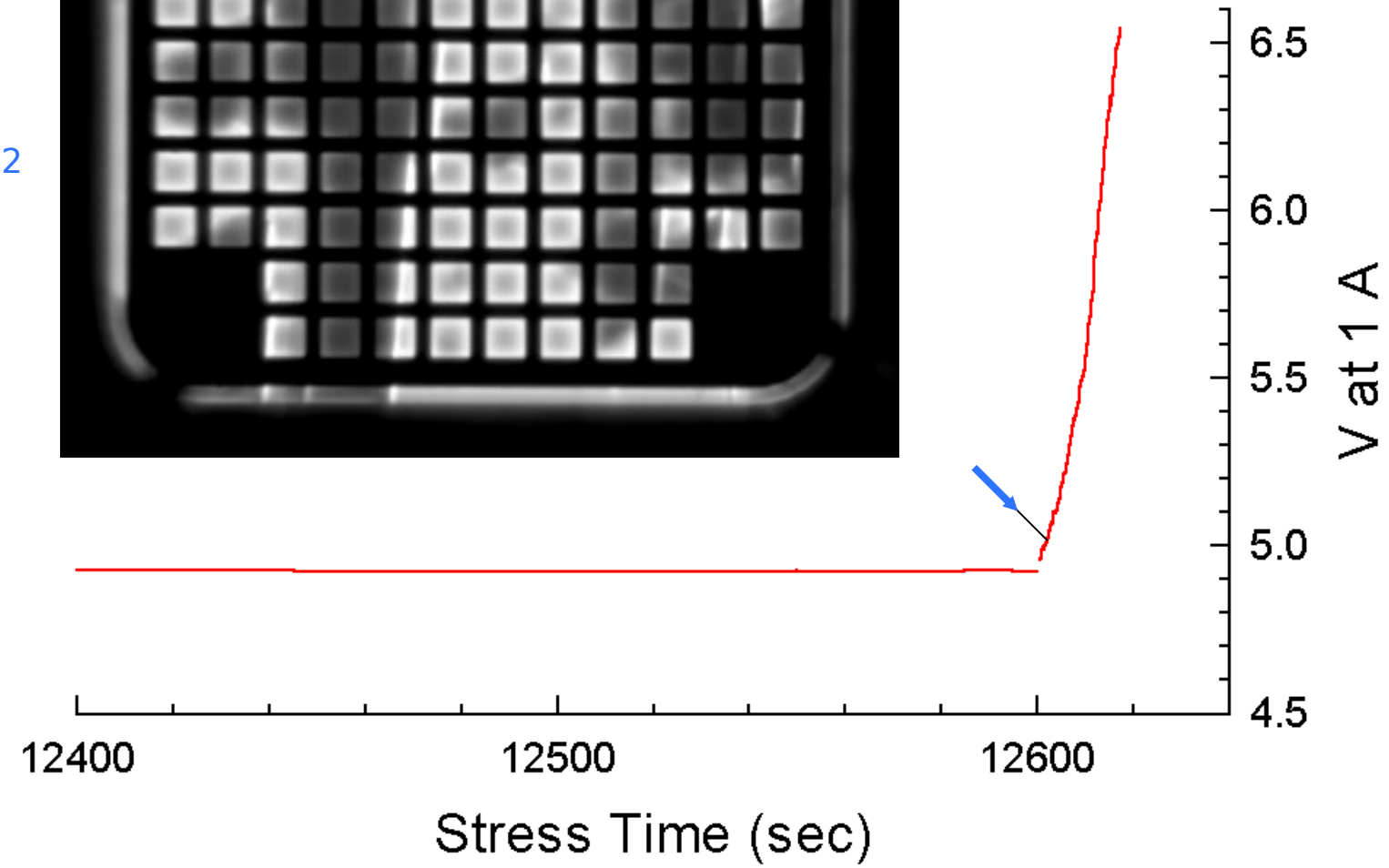
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



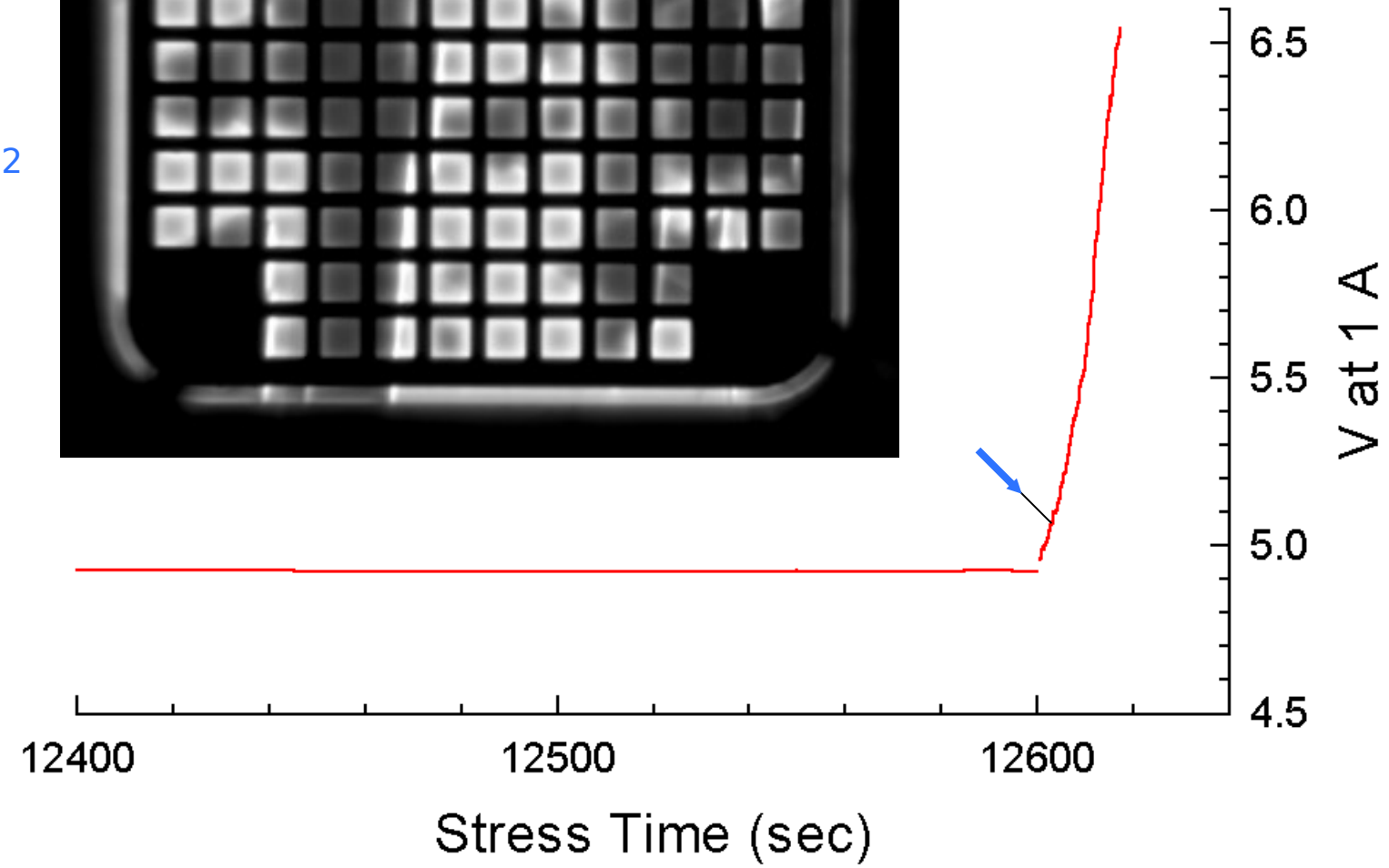
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



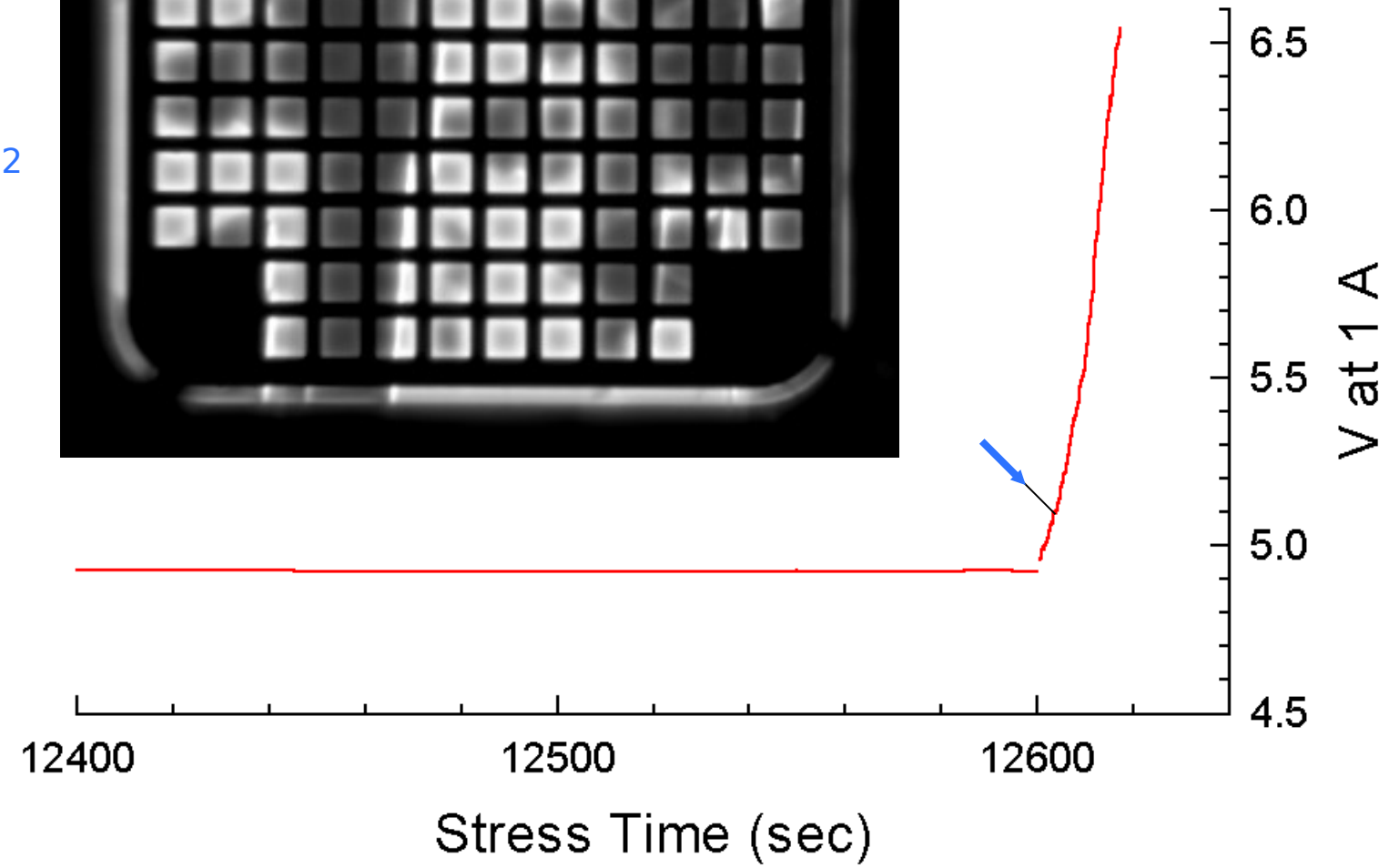
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



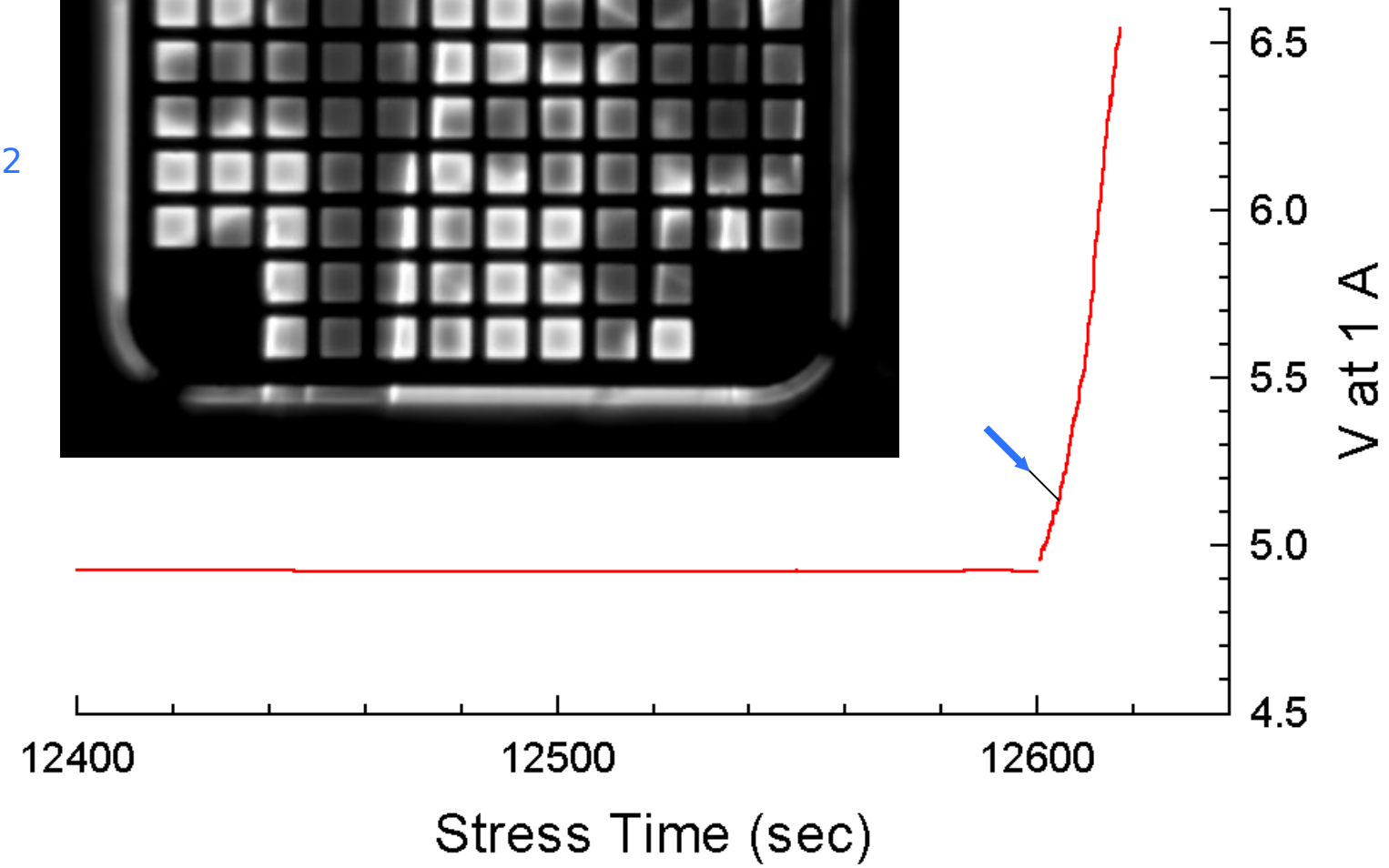
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



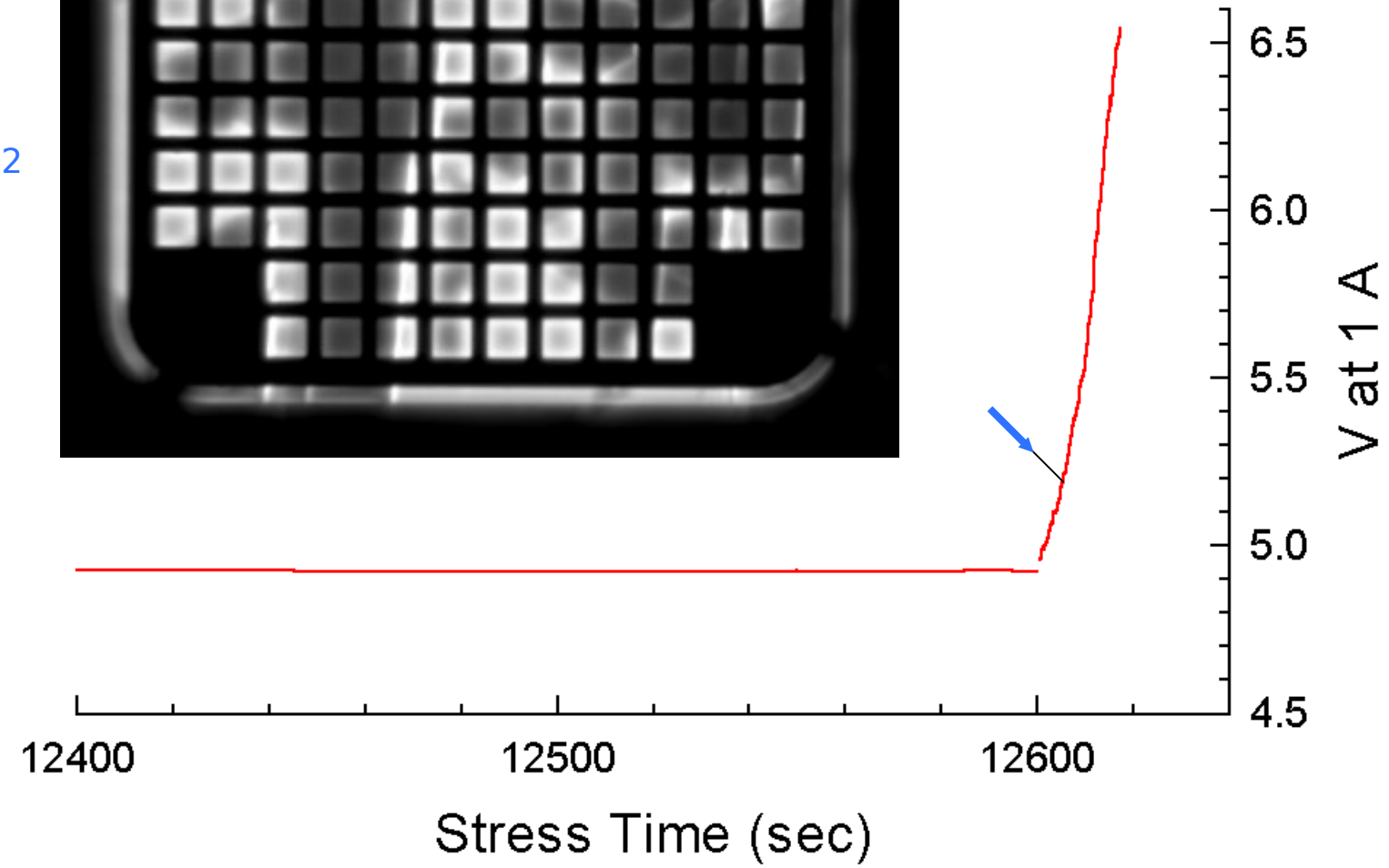
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



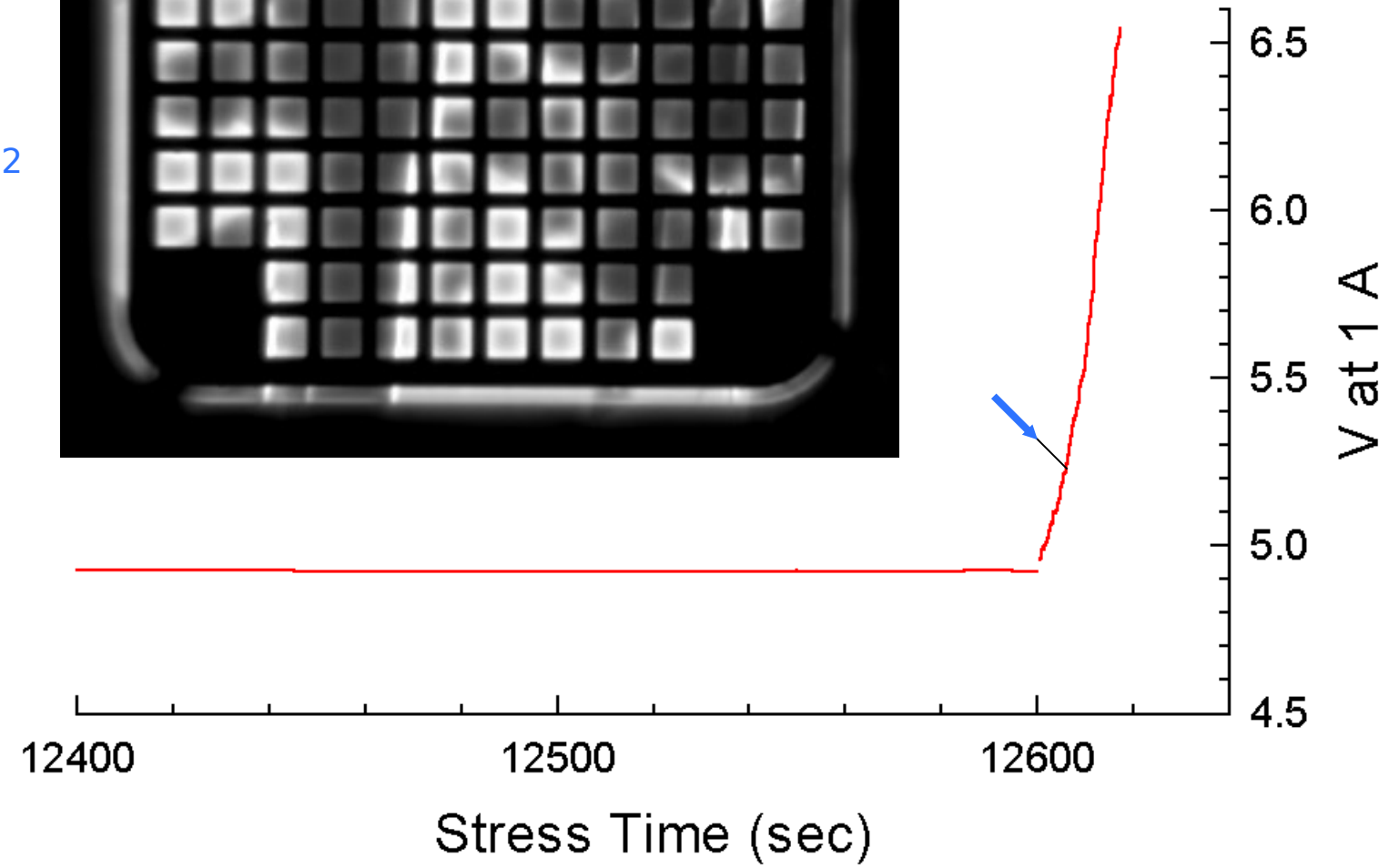
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



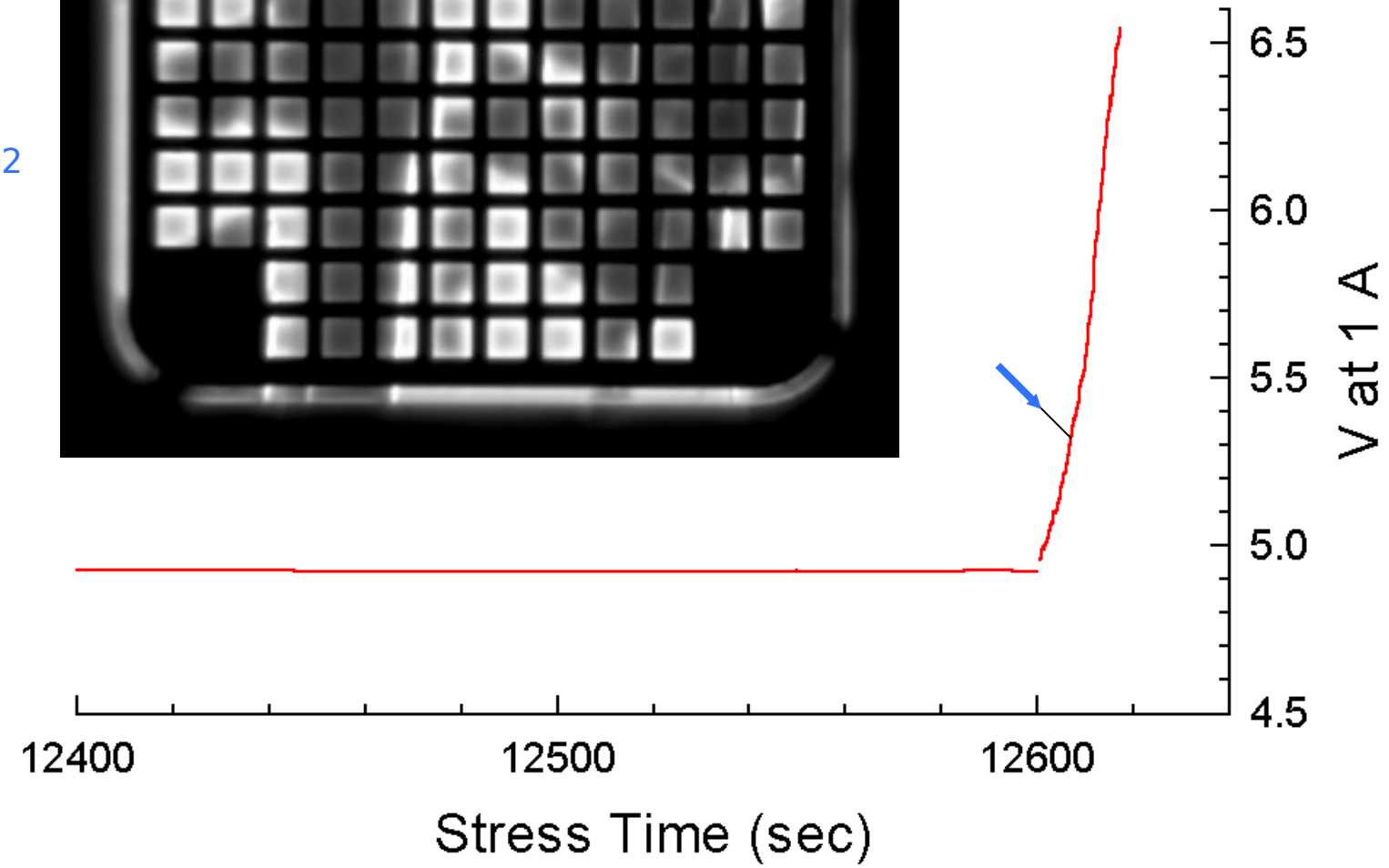
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



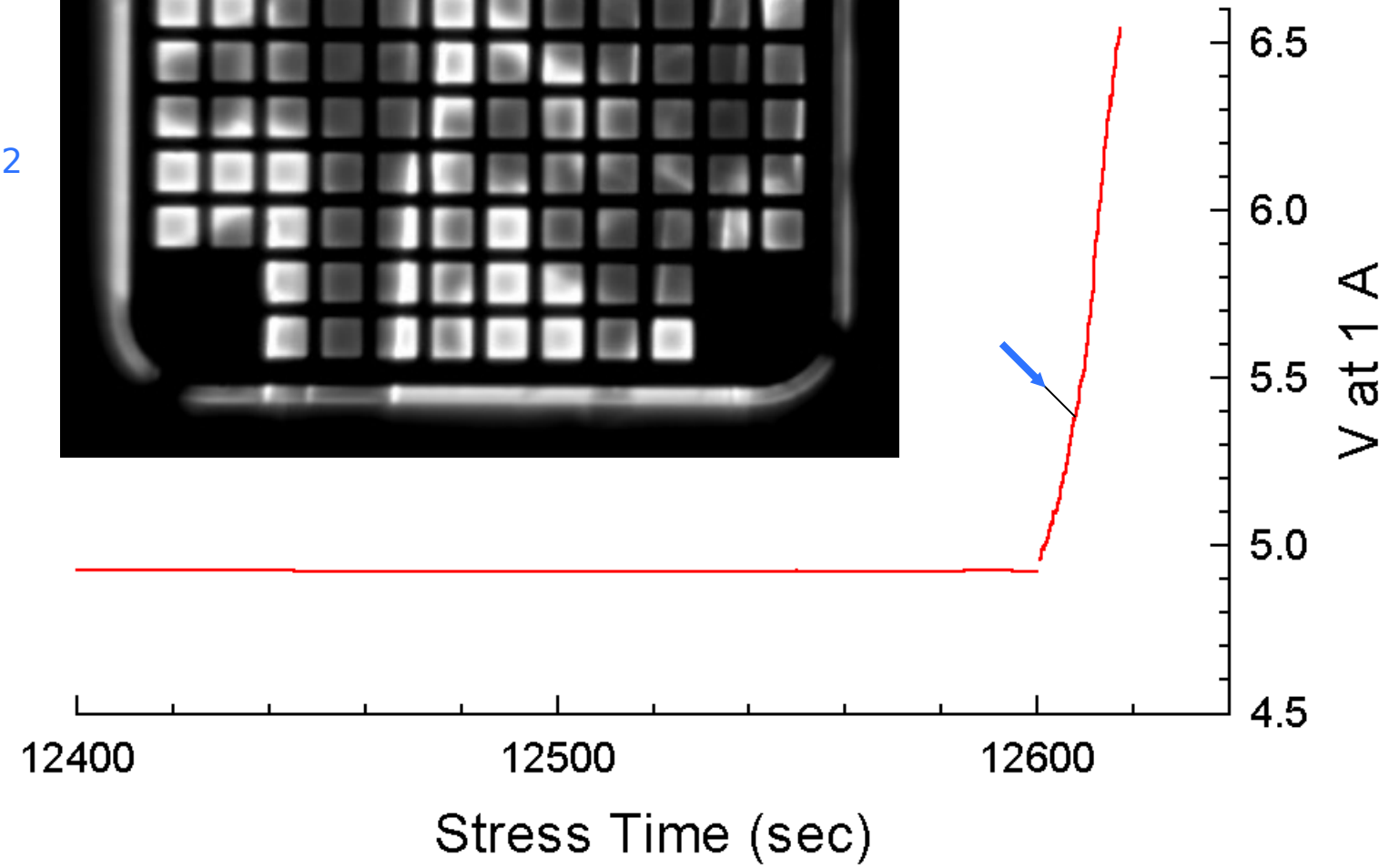
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



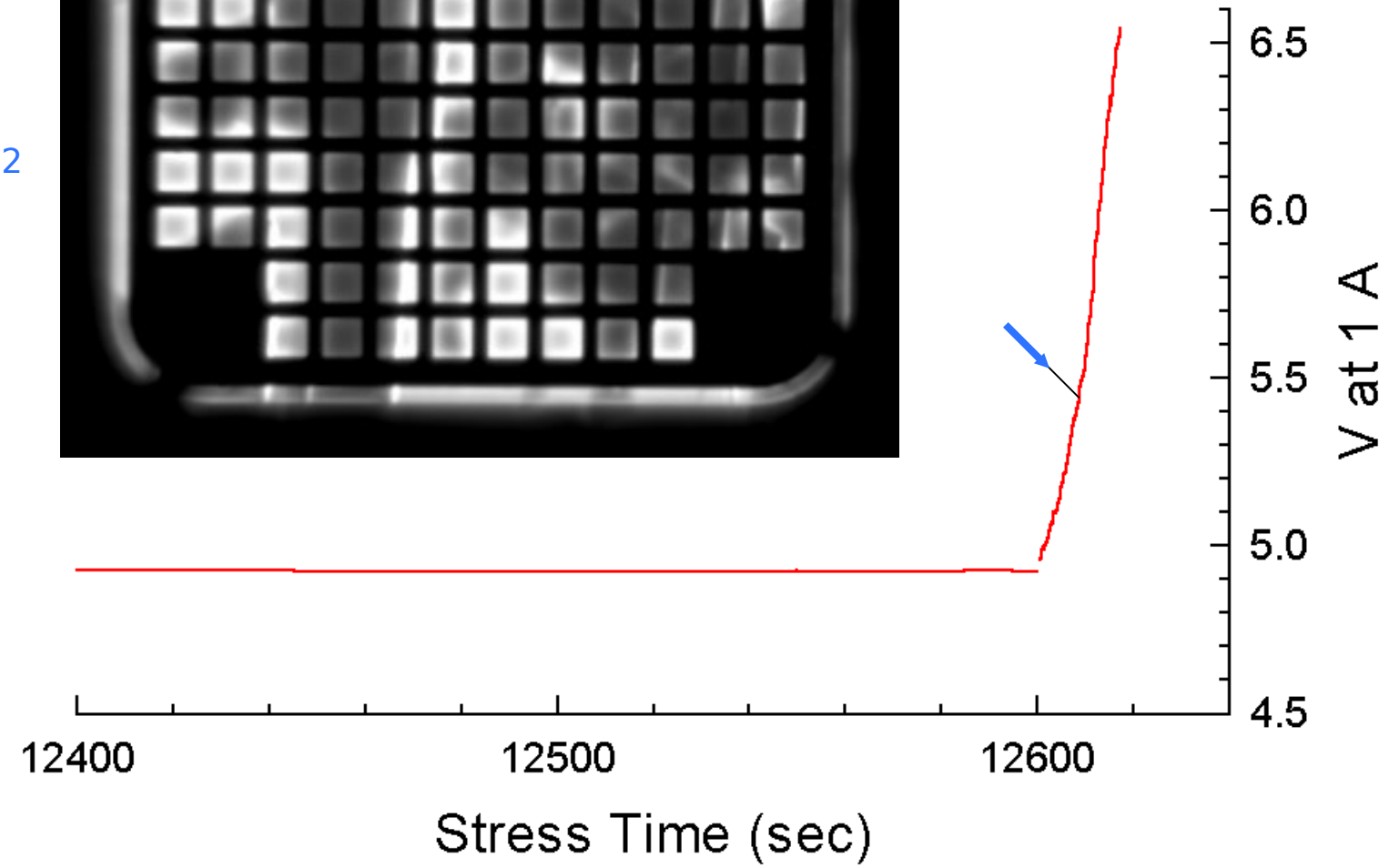
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



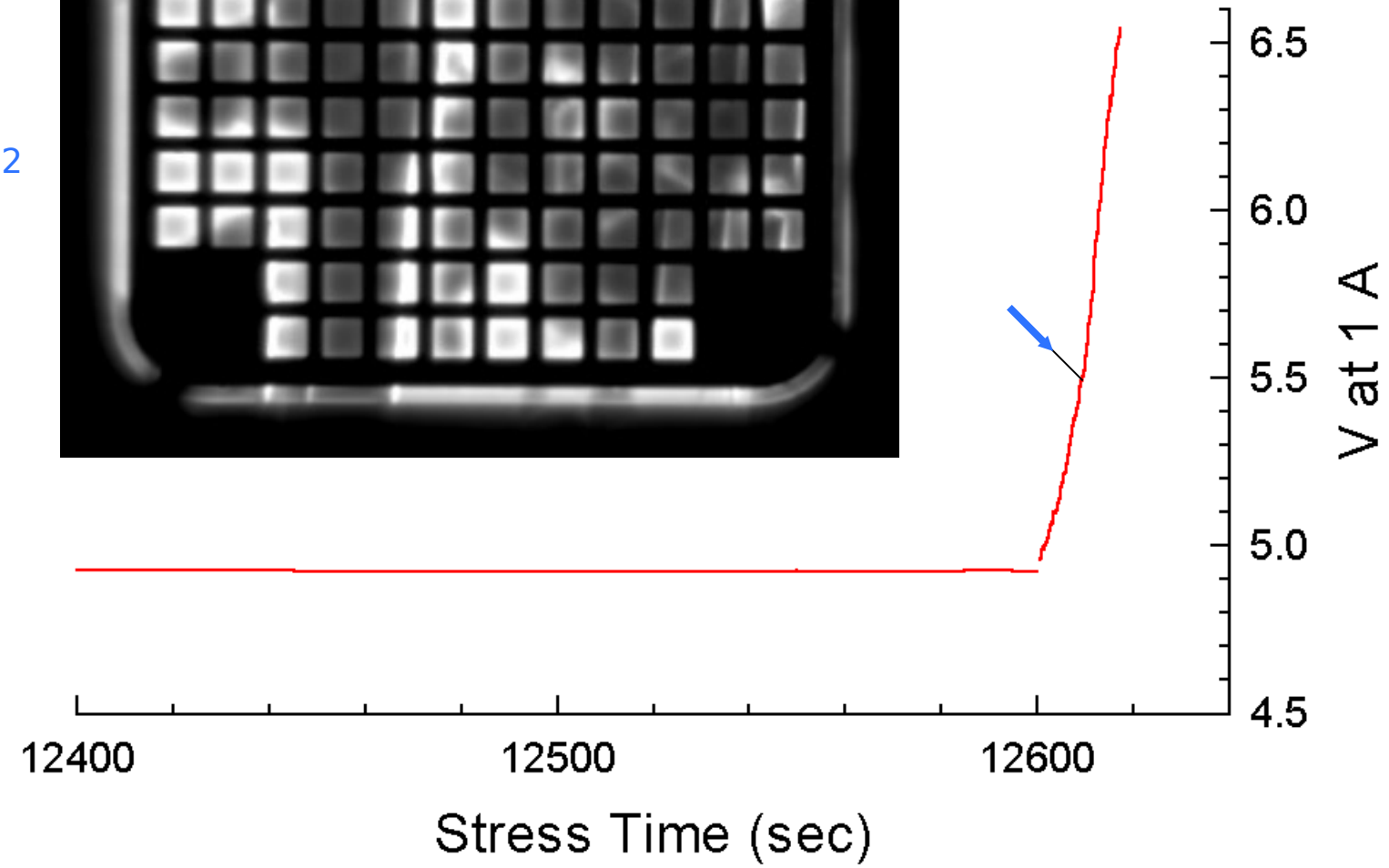
Diode

row 1 column 10

Current Stressing

10 A

1600 A/cm^2



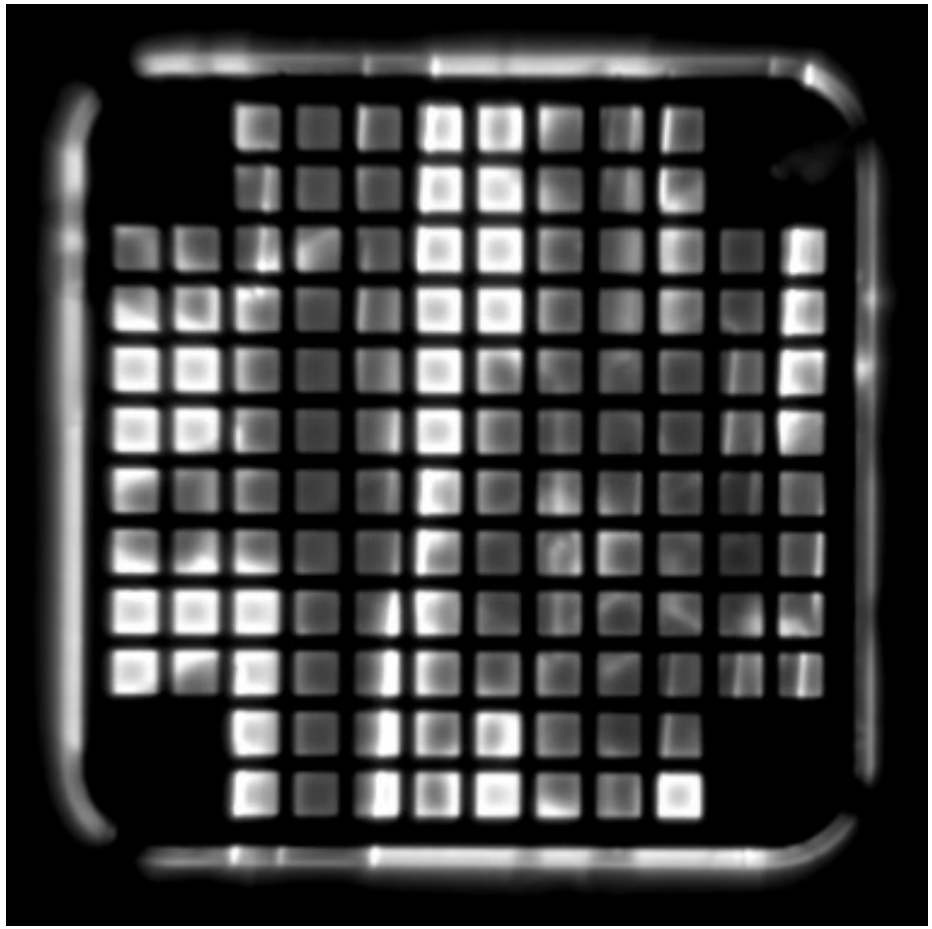
Diode

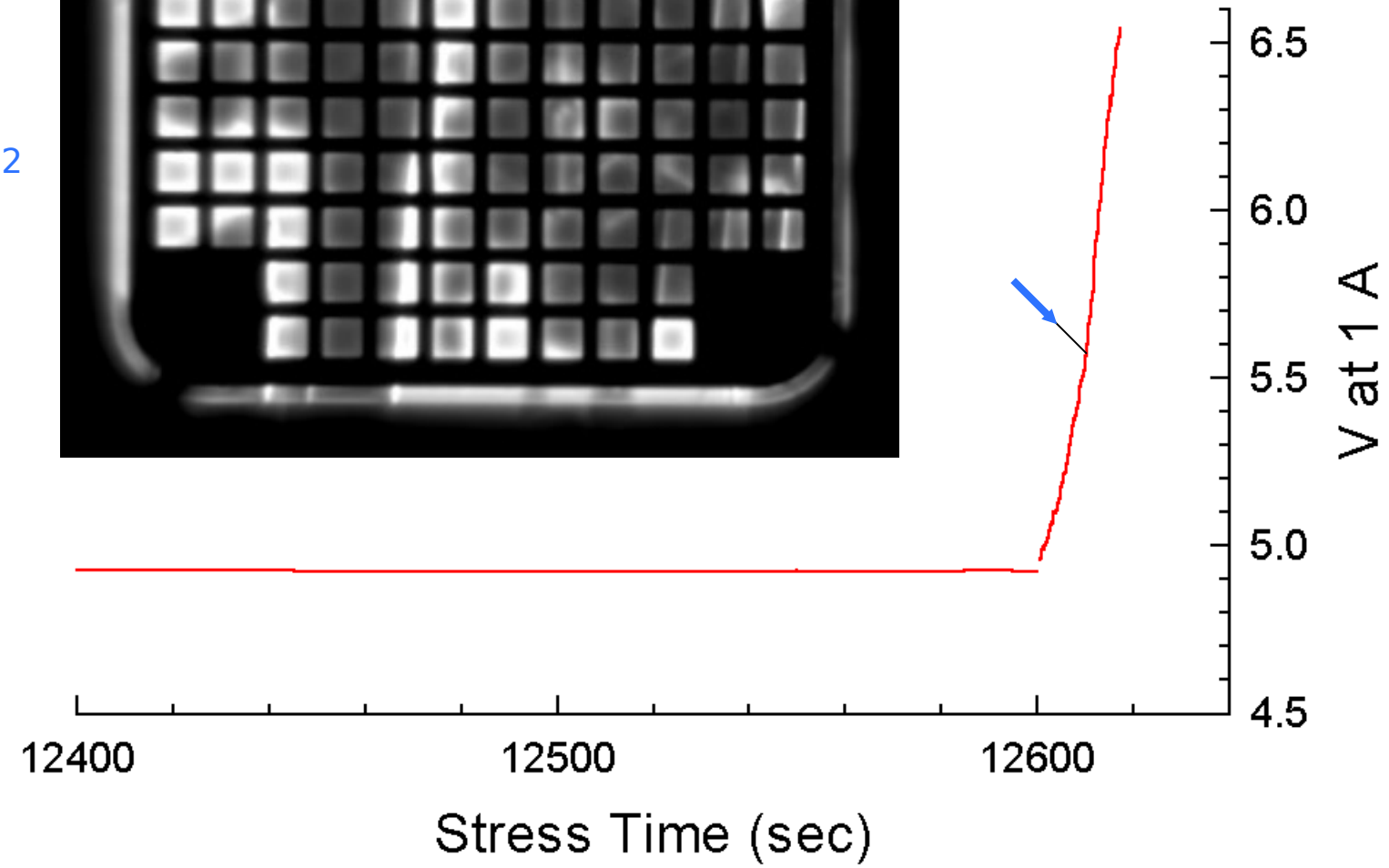
row 1 column 10

Current Stressing

10 A

1600 A/cm^2





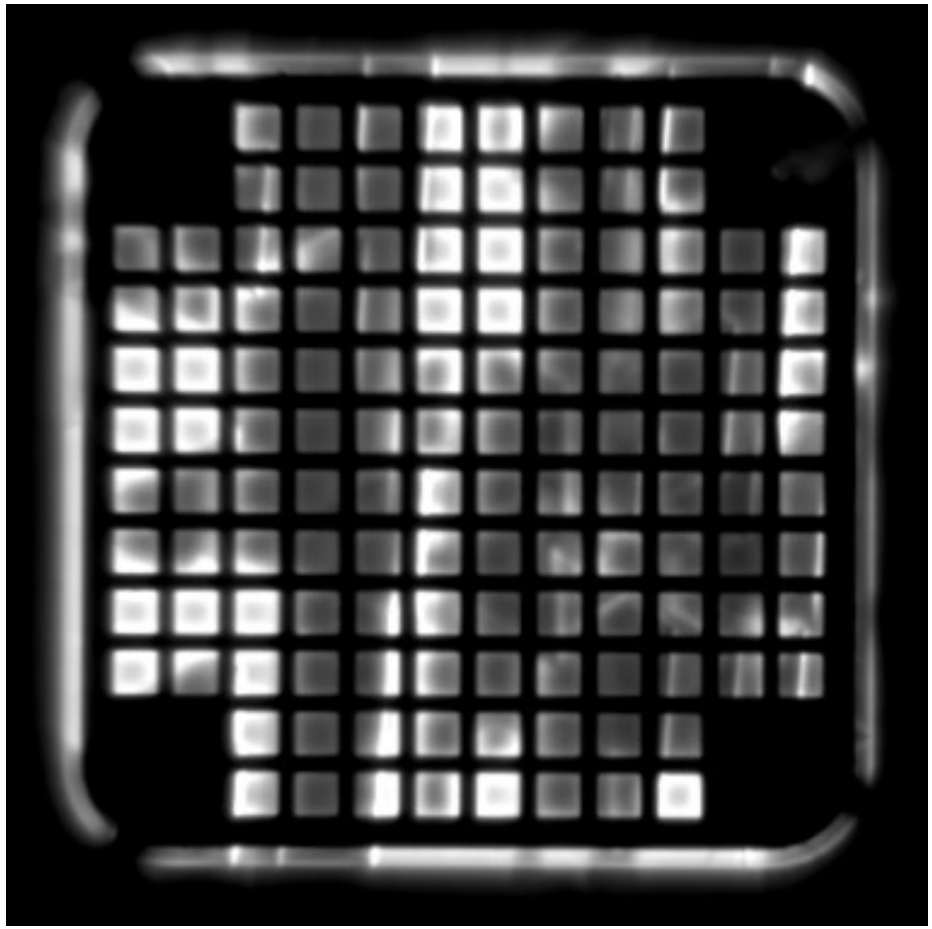
Diode

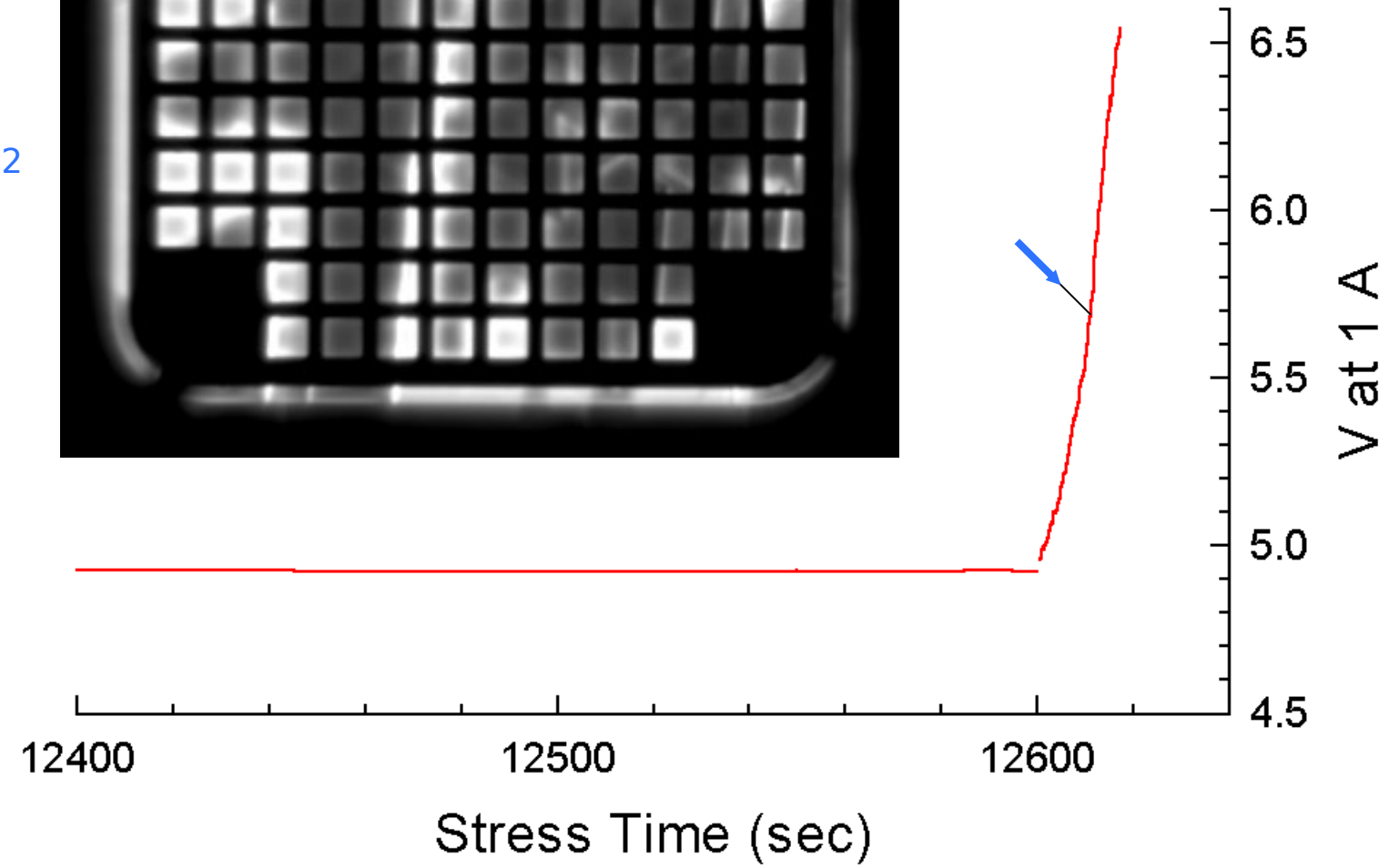
row 1 column 10

Current Stressing

10 A

1600 A/cm^2





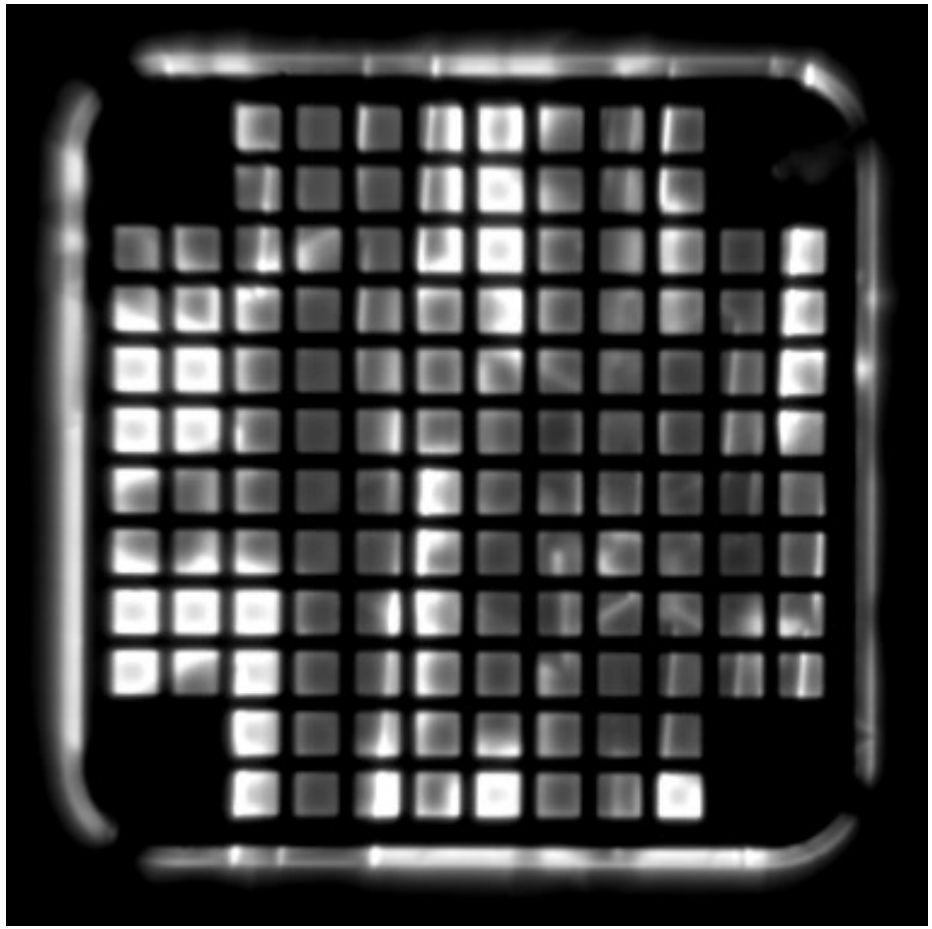
Diode

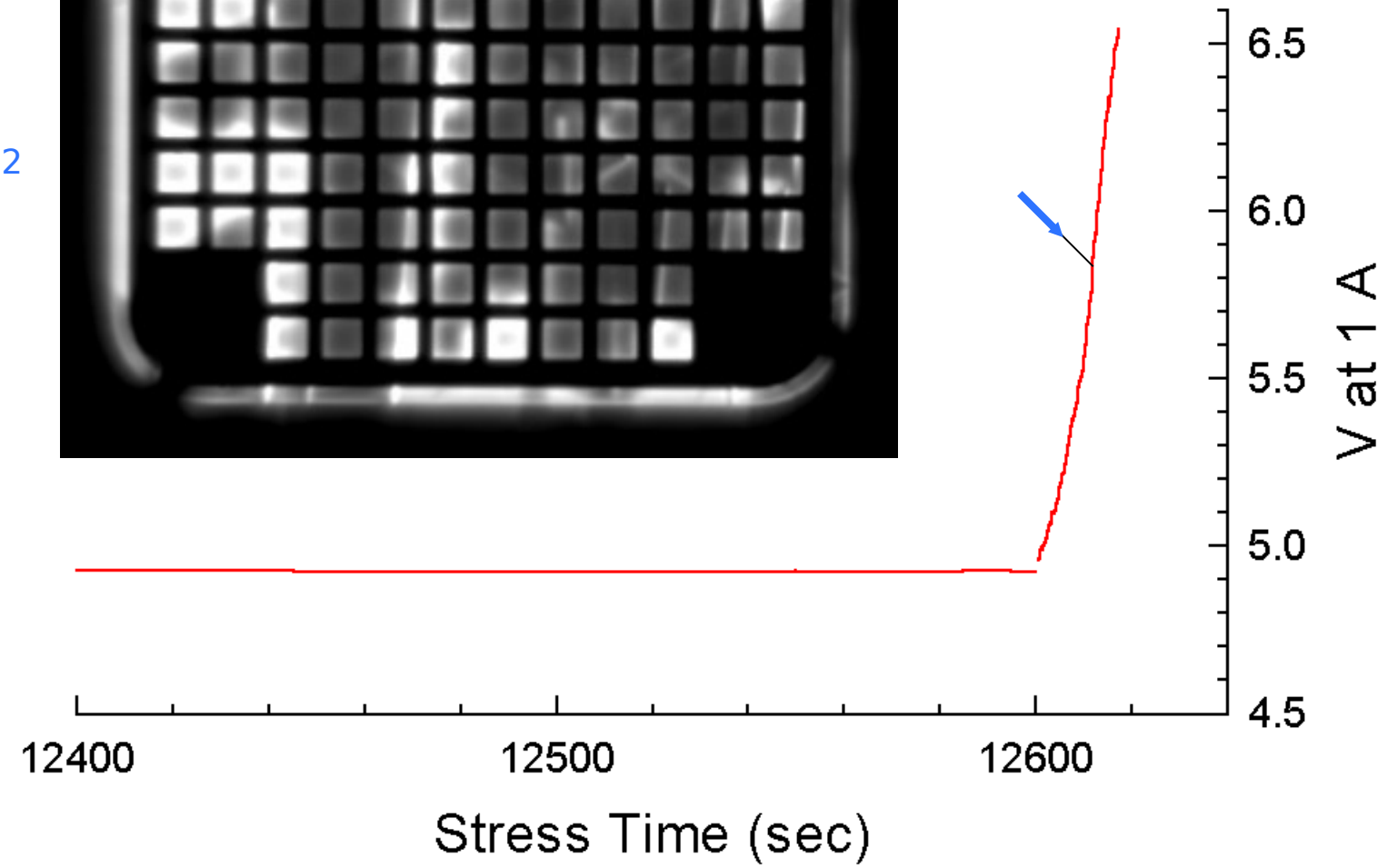
row 1 column 10

Current Stressing

10 A

1600 A/cm^2





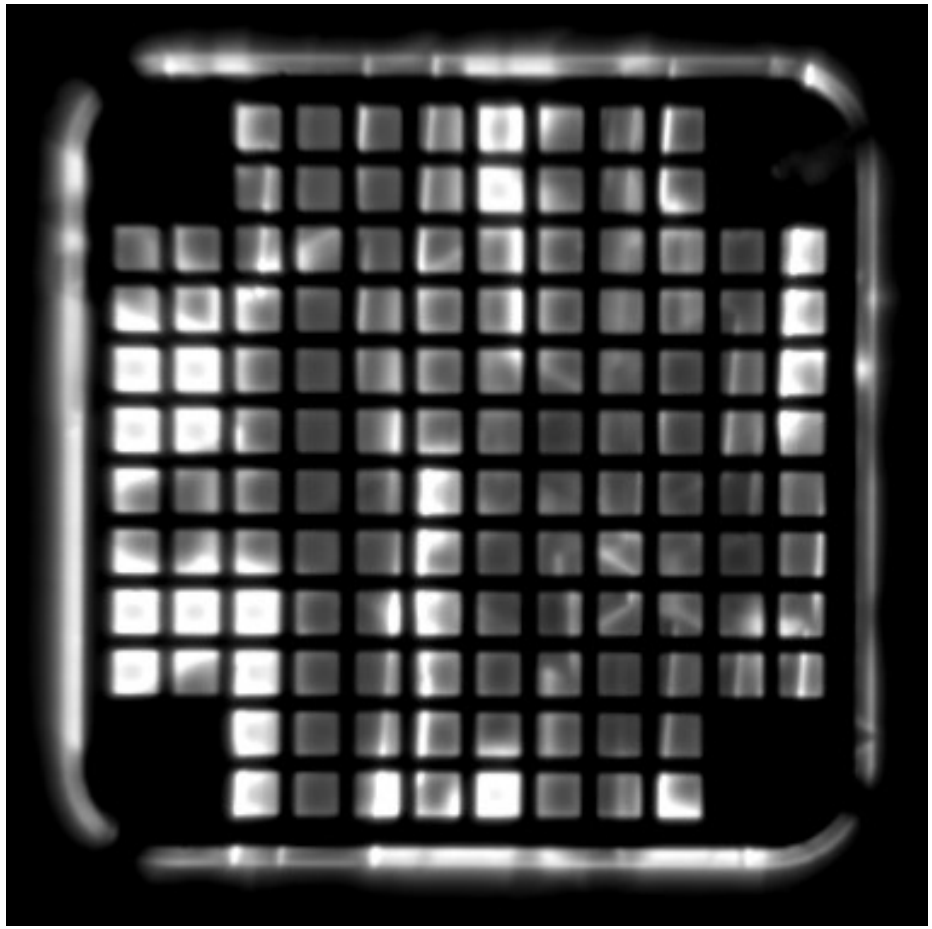
Diode

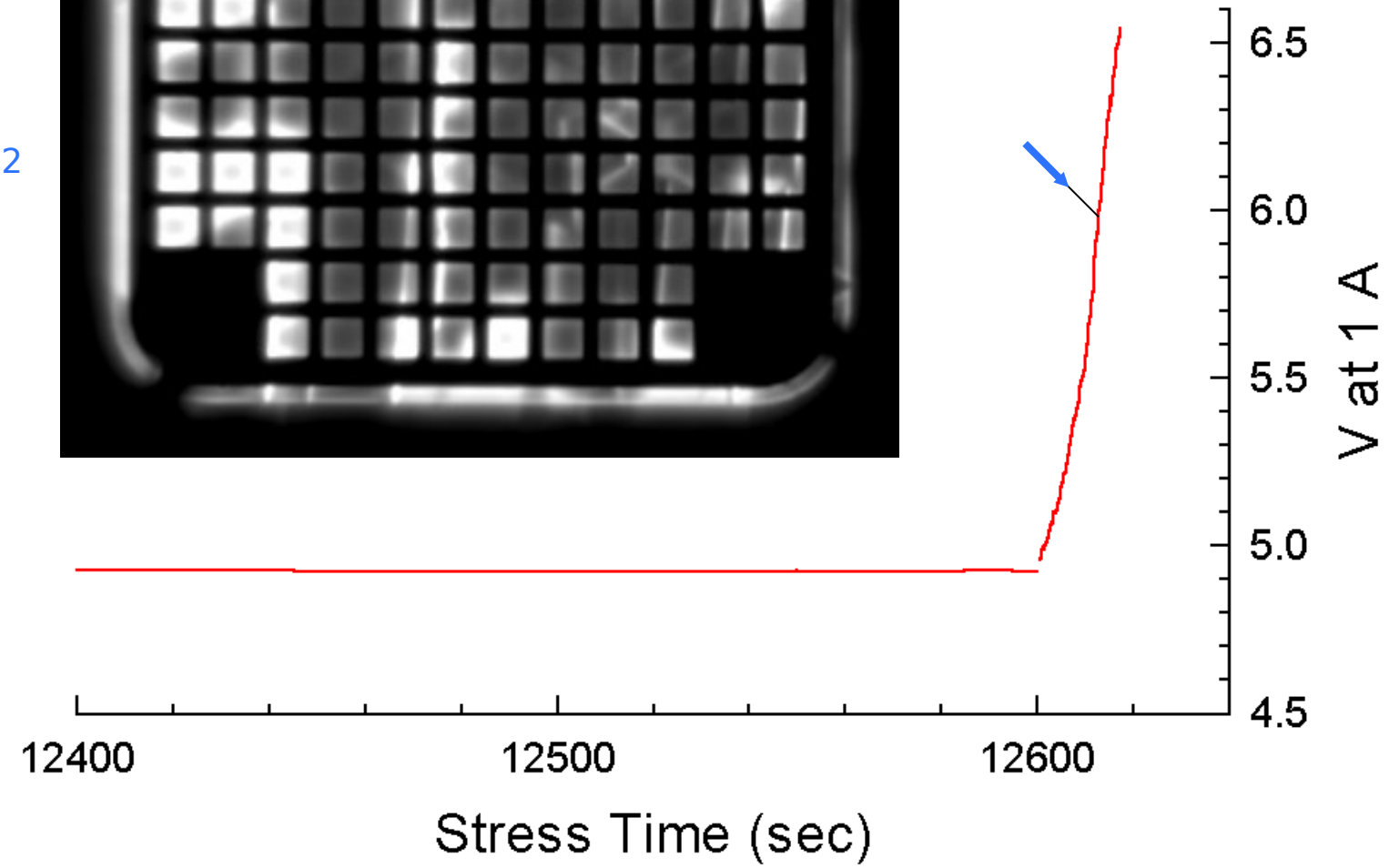
row 1 column 10

Current Stressing

10 A

1600 A/cm^2





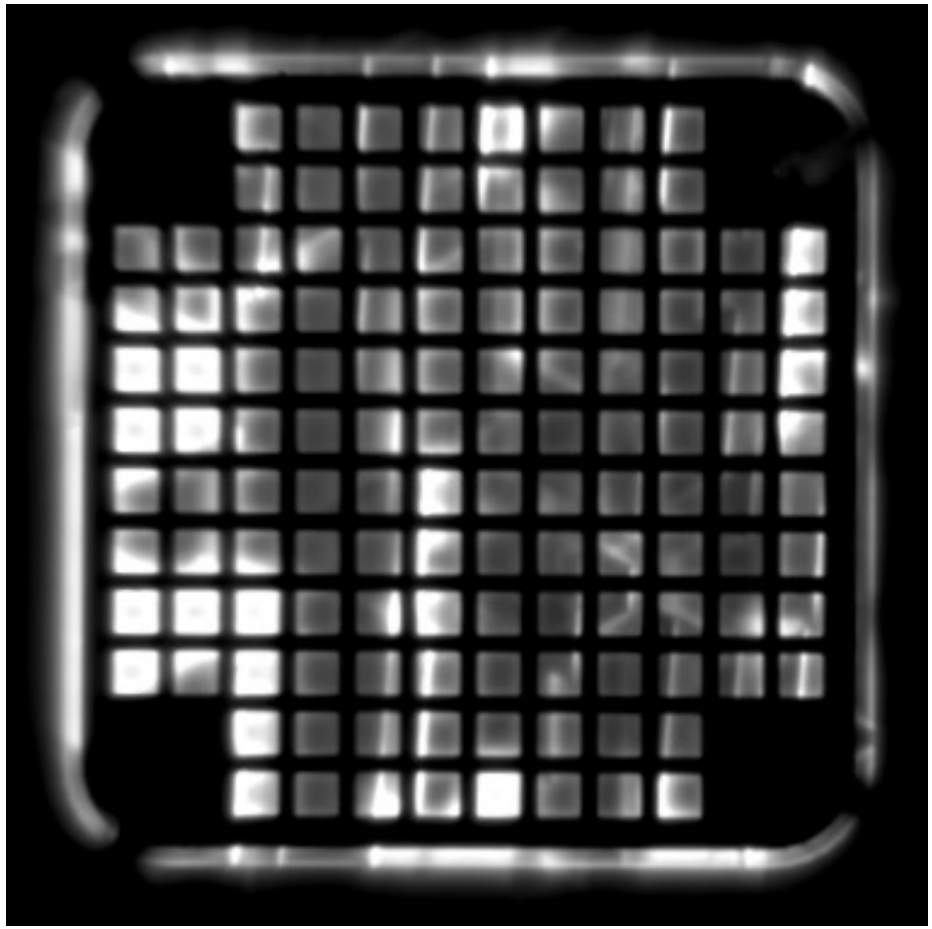
Diode

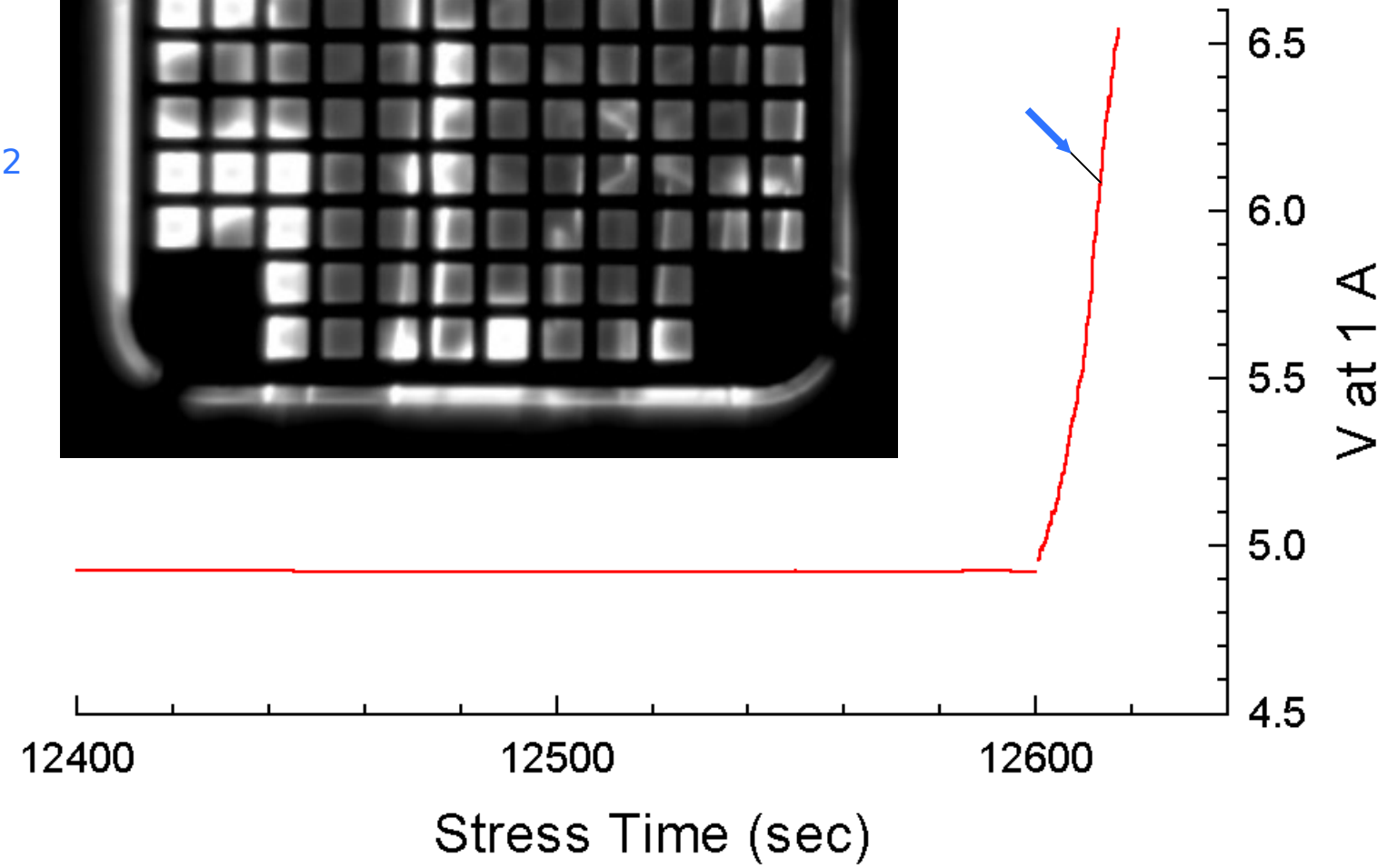
row 1 column 10

Current Stressing

10 A

1600 A/cm^2





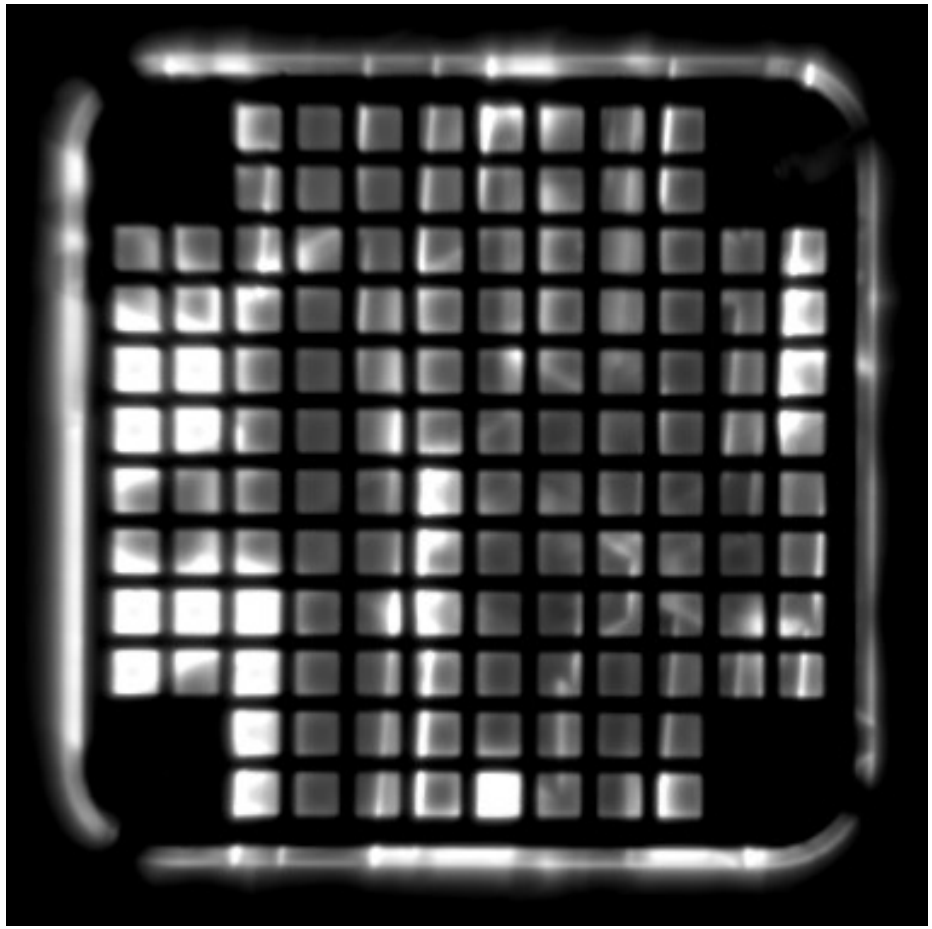
Diode

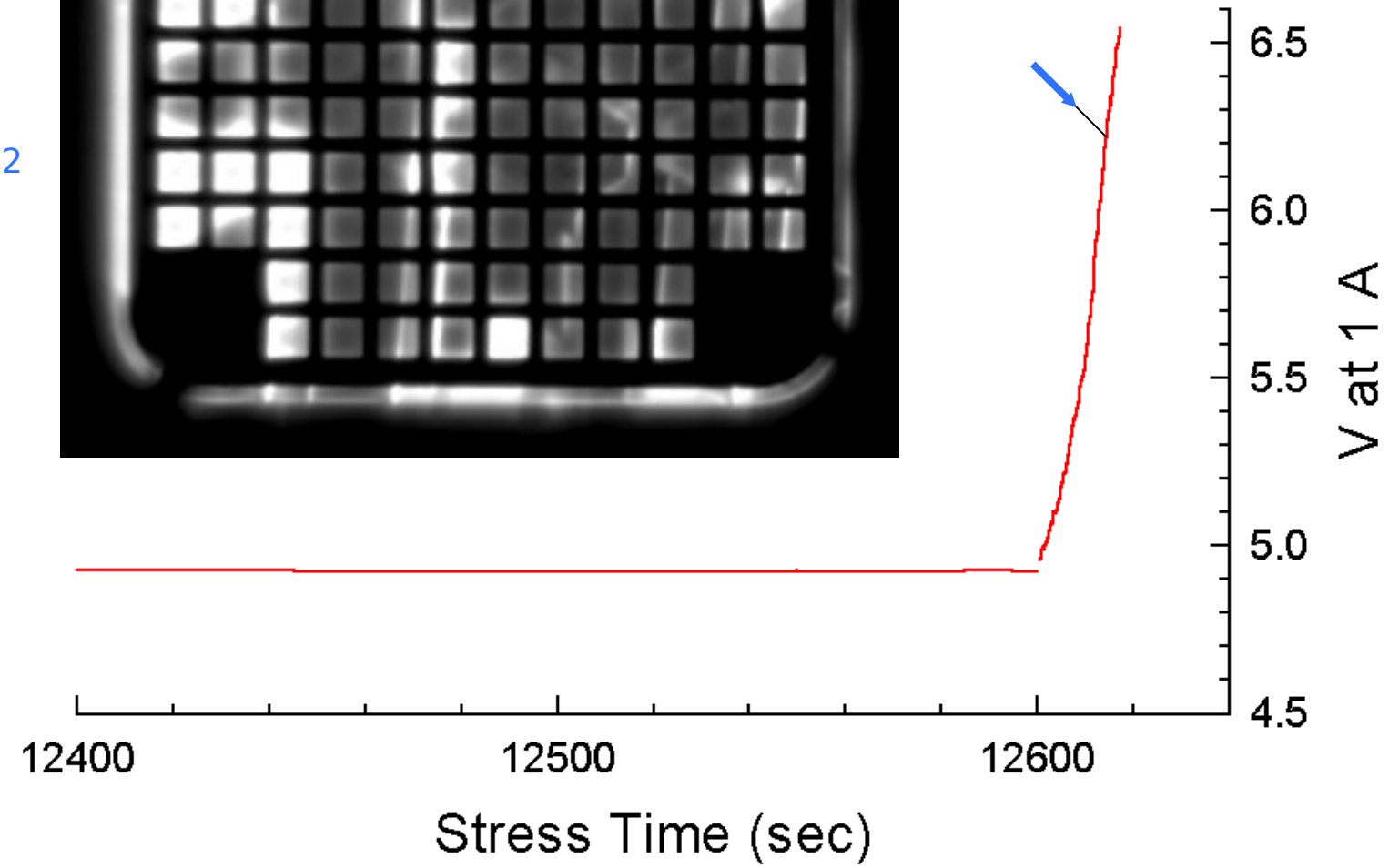
row 1 column 10

Current Stressing

10 A

1600 A/cm^2





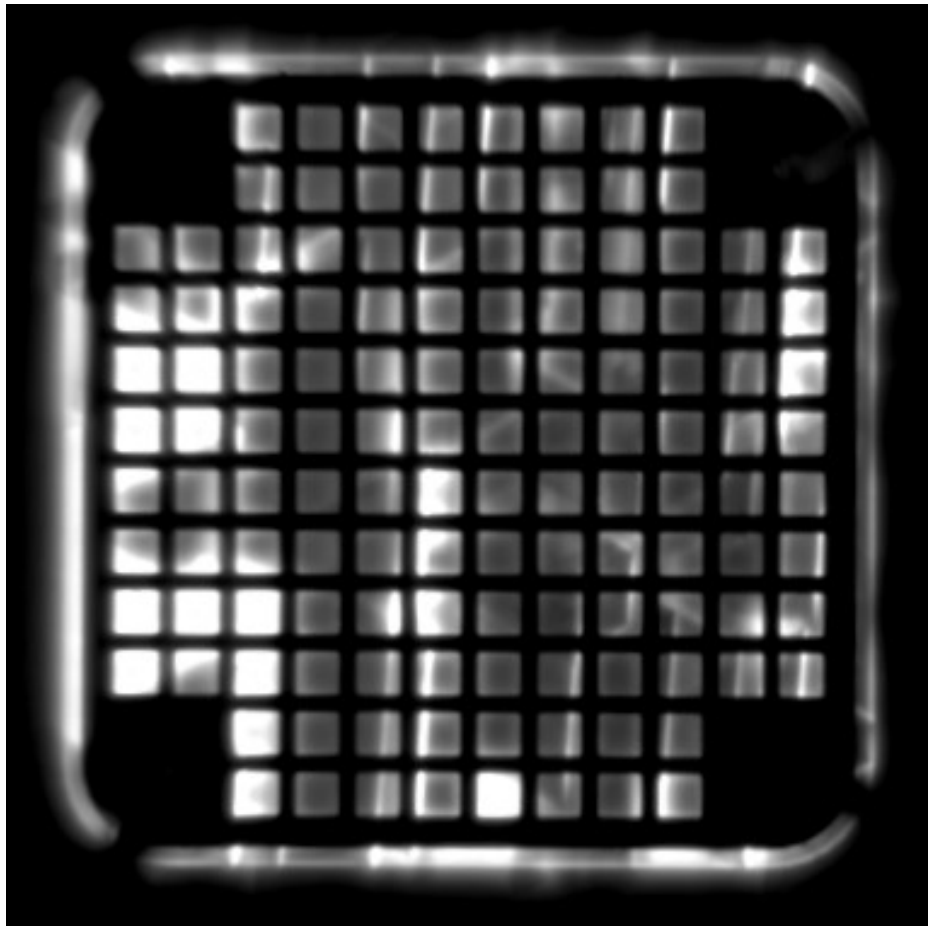
Diode

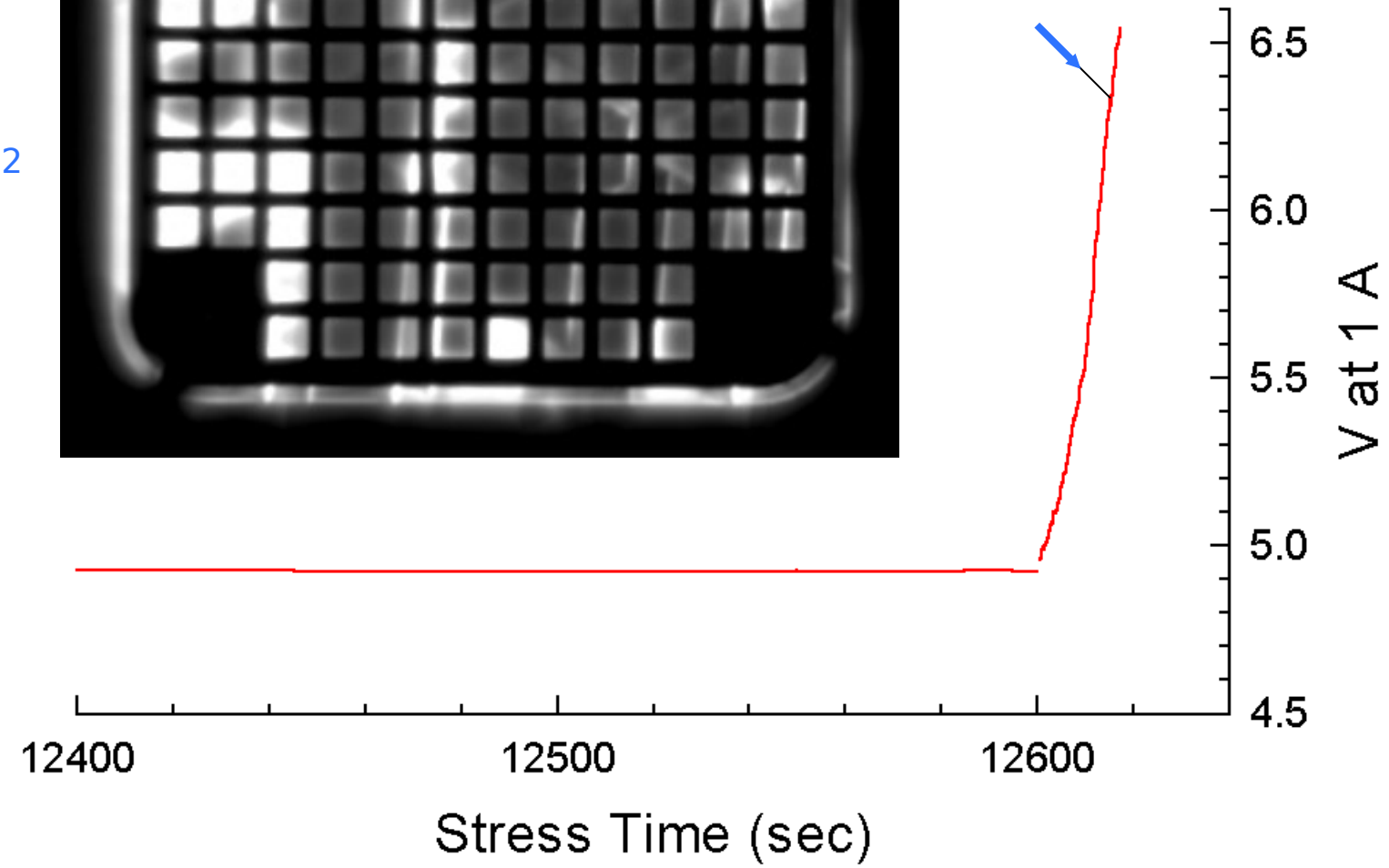
row 1 column 10

Current Stressing

10 A

1600 A/cm^2





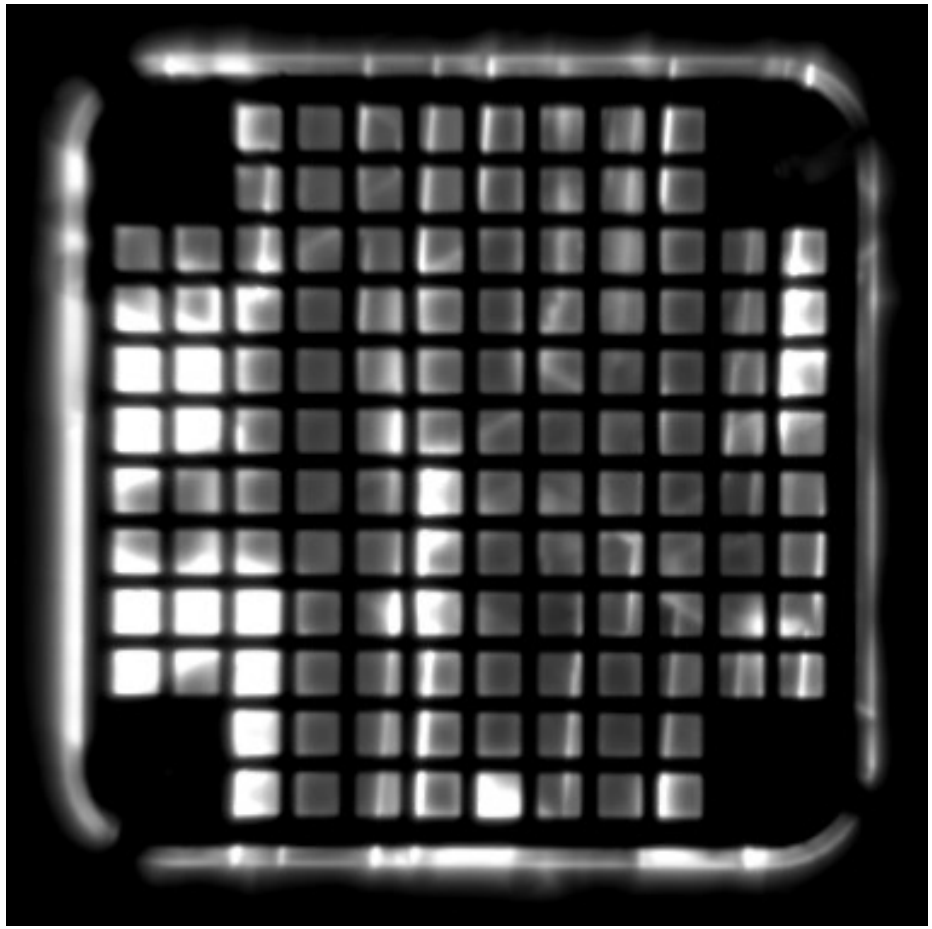
Diode

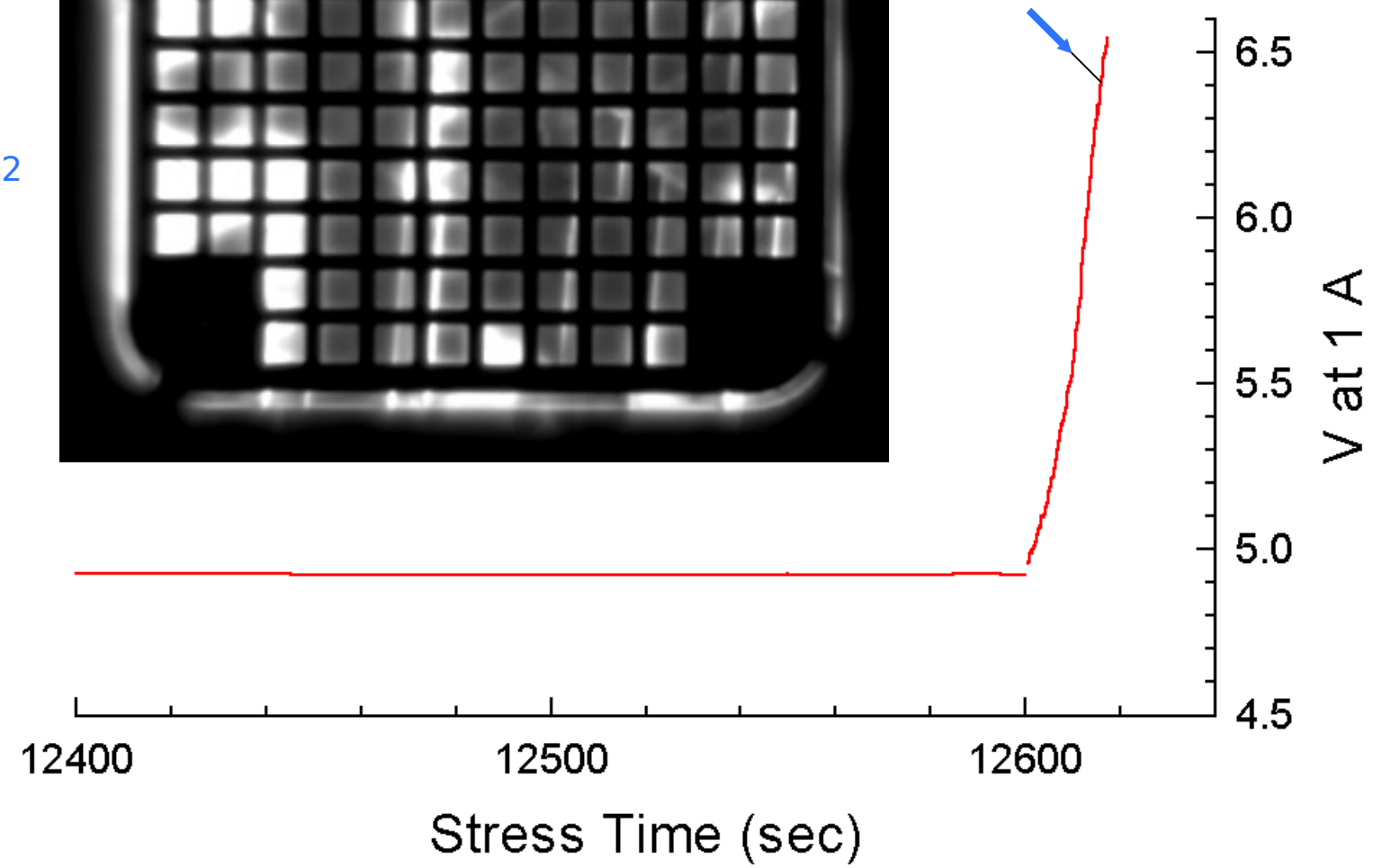
row 1 column 10

Current Stressing

10 A

1600 A/cm^2





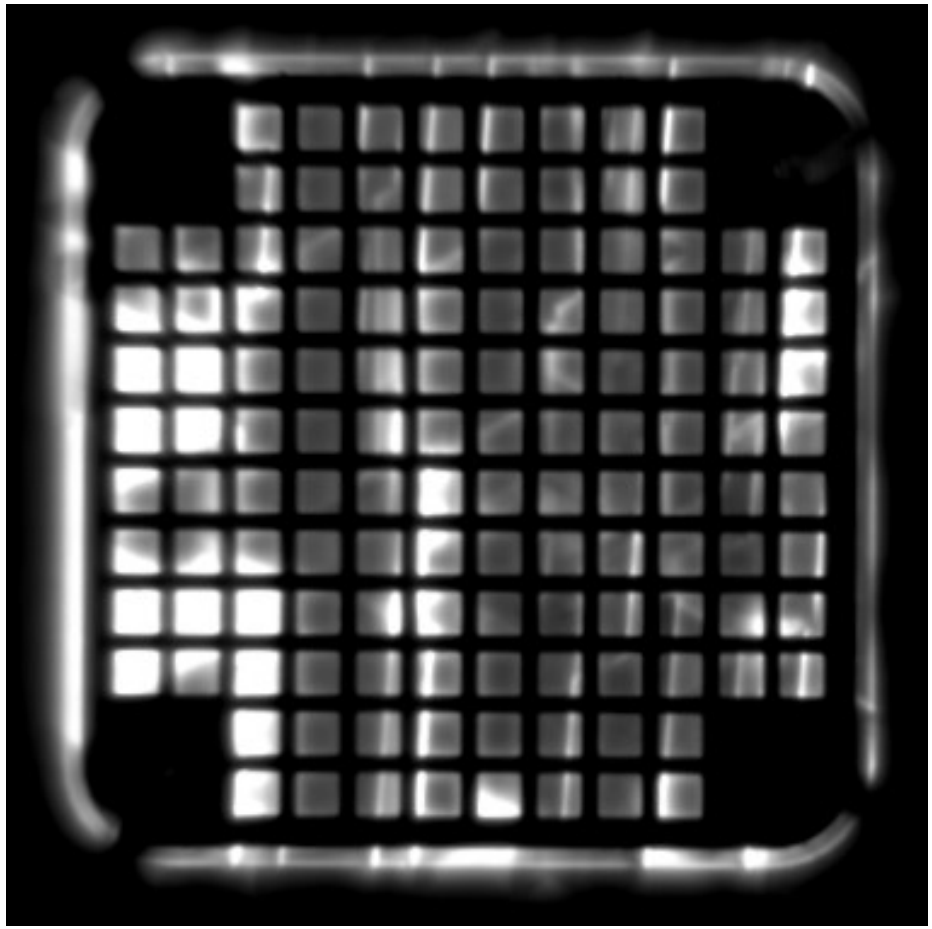
Diode

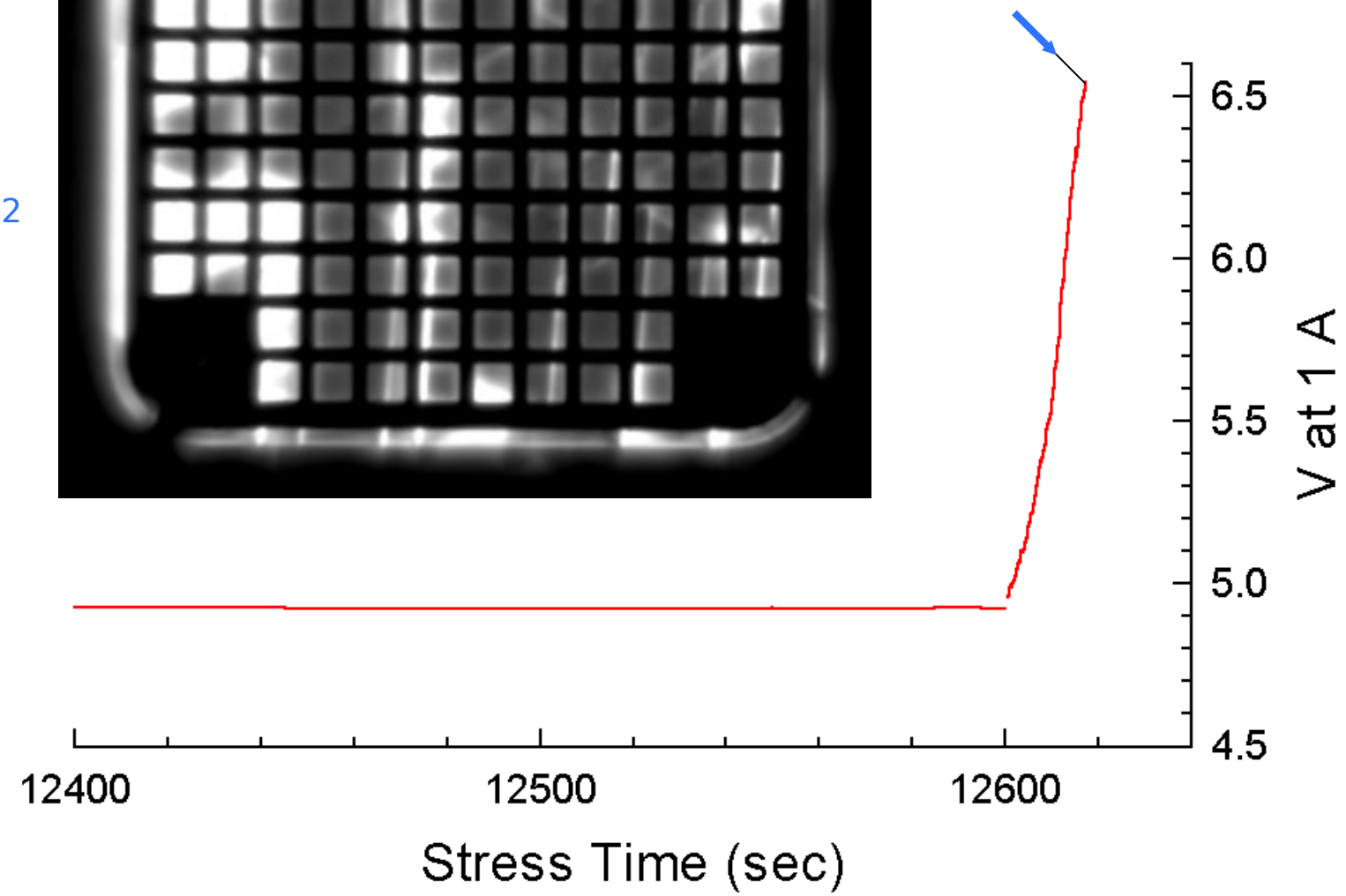
row 1 column 10

Current Stressing

10 A

1600 A/cm^2

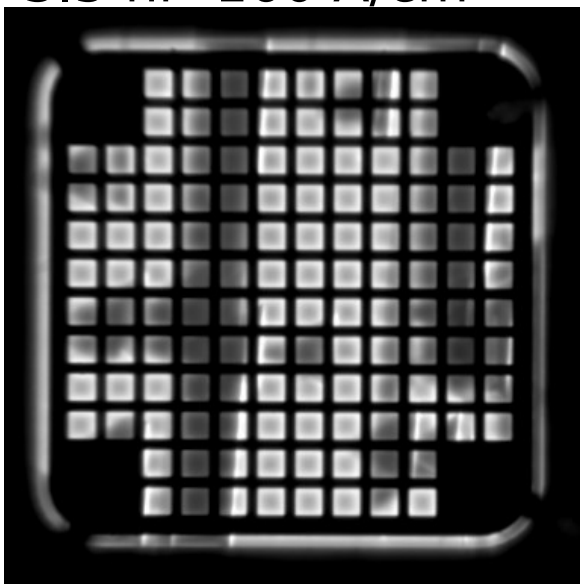




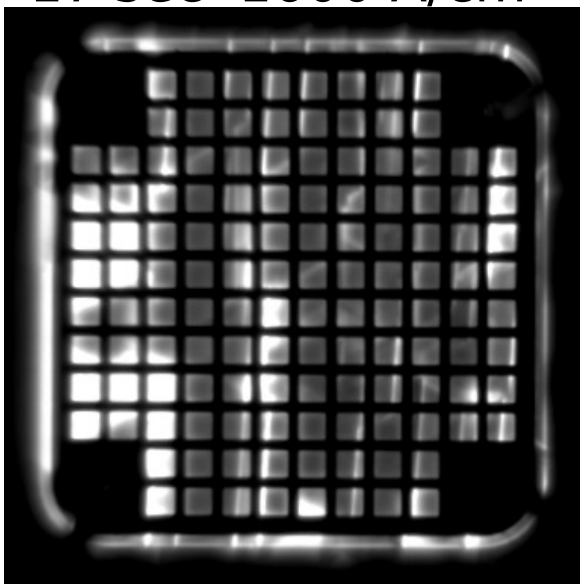
Comparing I-V Degradation

4.58 V @ 160 A/cm²
before stress

4.93 V @ 160 A/cm²
3.5 hr 160 A/cm²



6.55 V @ 160 A/cm²
17 sec 1600 A/cm²



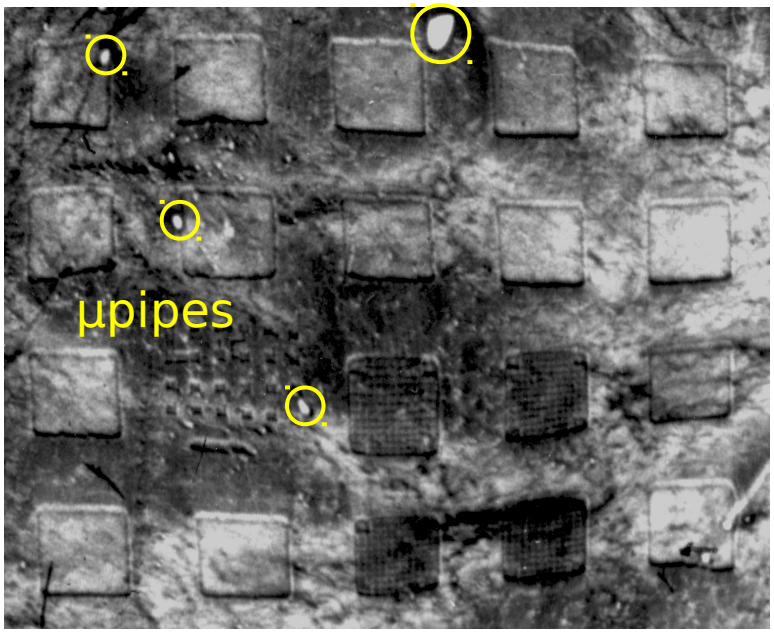
After increasing current density (T < 120°C):

1) Pinned stacking faults start growing

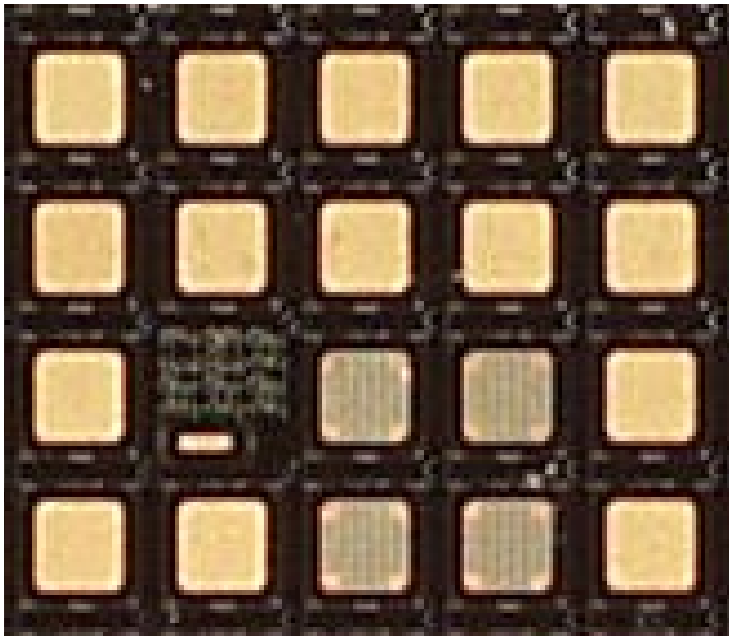
2) New stacking faults start growing

Lattice Plane Distortions

X-ray topograph of diodes



Picture of processed diodes

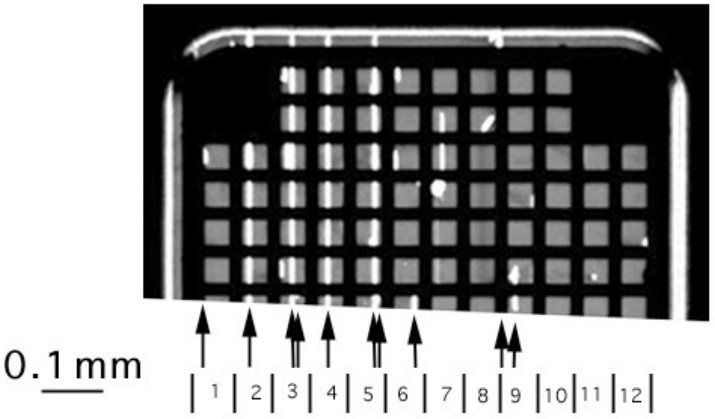


Distortions due to spatially varying stress

Site-Specific TEM

One-to-one correspondence between LEI and TEM

Light Emission Image



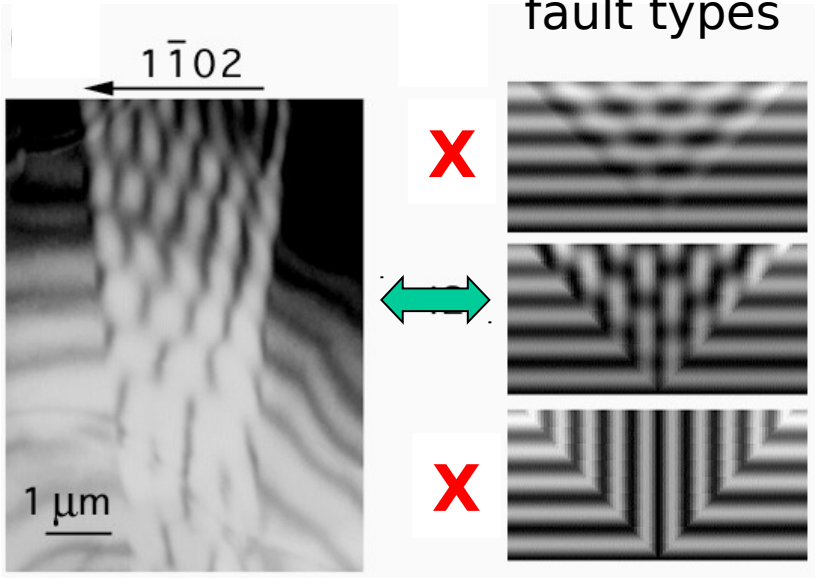
Locations of stacking faults identified by TEM

Determining stacking fault type by comparing TEM images to simulations

Shockley fault → Stress-induced

TEM image

Simulations for fault types



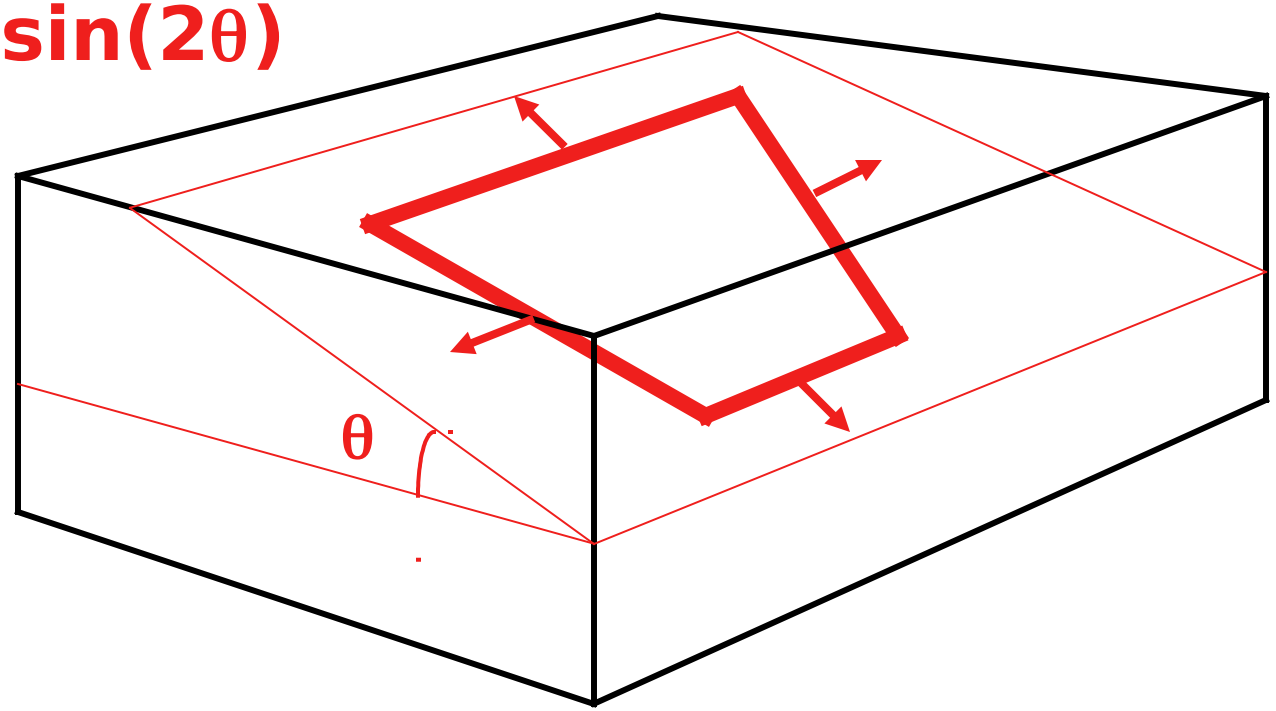
Conclusions about Stacking Fault Growth

- Stacking faults nucleate throughout the thickness of the epitaxial layer
- Preliminary investigation of nucleation sites - consistent with basal plane dislocations
- Role of strain:
  Stress both drives stacking fault formation and pinning
  Complex growth dynamics of stacking faults
  due to varying stress - fractal-like nature

Approach to Decreasing the Driving Force for Stacking Fault Growth

Decrease the tilt angle θ to decrease the forces on partial dislocations bounding the stacking fault for SiC film under tension or compression

$F_{partial} \sim \sin(2\theta)$



Progress Towards Solving the Stacking Fault Problem

- Developed unique and powerful combination of physical characterization capabilities
- Beginning to identify nucleation sites using LEI, site-specific TEM and x-ray topography
- Identified complicated role mechanical stress plays in stacking fault formation
- Working with state-of-the-art SiC wafer and device vendors